Chapter 15

ARM – Architecture, Programming and Development Tools

Lesson 07

ARM Cortex CPU and Microcontrollers

Microcontroller CORTEX M3 Core

32-bit RALU, single cycle MUL,
2-12 divide, ETM interface,
control logic,
Thumb decoder,
Thumb-2 decoder

Bus Matrix
(Multiple 32-bit
buses)

Interface for NVIC

Memory Protection

Nested Vector Interrupt
Controller

FPB

DWT

Debug Port
SerialWire/

JTAG

Interfaces to
SRAM, Peripherals
and Code Memory

Timer

Real Time
System clock
Interrupts

http://www.arm.com/pdfs/Cortex_M3_DS.pdf

Microcontroller CORTEX M3 Core

32-bit RALU, single cycle MUL, DSP, Floating Point Unit, 2-12 divide, ETM interface, control logic, Thumb decoder, Thumb-2 decoder

WIC

Bus Matrix (Multiple 32-bit buses)

Interface for NVIC

Memory Protection

Nested Vector Interrupt Controller

FPB

DWT

Debug Port SerialWire/ JTAG

Interfaces to SRAM, Peripherals and Code Memory

Timer
Real Time
System clock
Interrupts

http://www.arm.com/products/processors/cortex-m/cortex-m4-processor

Features

- http://www.arm.com/pdfs/Cortex_M3_DS.pdf
- Small core footprint [— number of gates used in the core for similar instruction set of the core]
- High code density—requires smaller memory for the code
- Small pin count.
- Low power consumption.
- Harvard memory architecture.

Features

- Excellent integration of the peripherals/SRAM through memory protection unit.
- Three-stage pipeline with branch prediction.
- Single cycle multiply.
- Two to twelve cycle signed/unsigned divide.
- Unaligned data storage programmability.

Features

- Atomic bit manipulation—instructions are required for wireless networking and serial transmissions of the bits. [Atomic means interrupt only after completing the bit manipulation.]
- Supports sleep modes
- 1.25 Dhrystone MIPS per MHz clock cycle
- Thumb®-2 instruction set architecture

Features

- Debug port configurable by SerialWire or JTAG
- DWT [data watch points (break points) and trace]
- FPB (flash path and break point unit)
- Six program breakpoints
- Two data-fetch break points.
- ETM (embedded trace macrocell) interface—for tracing the real-time instructions.

NVIC (nested vectored interrupt controller)

1. Nesting (stacking) of interrupts for Exceptional system response mechanism for the interrupts
2. Interrupt of low priority can be preempted by exerting higher priority
3. Supports dynamic re-priority allocations
4. Interrupts that are being serviced are blocked from further activation until the interrupt service completes

Interrupt latency

- 12 cycles in contrasts to ARM 7, which has 24 to 42 cycles of interrupt latency
- Excellent deterministic interrupt behaviour
- NVIC integrates with the timer for the system ticks
- 24-bit count-down timer
- Generates interrupts at regular time intervals It thus gives system clock to run RTOS and timer for scheduling the tasks.

Timer

- 24-bit count-down timer
- Generates interrupts at regular time intervals
- System clock to run RTOS
- System clock for scheduling the tasks

Features

- Support Jazelle RCT (Runtime Compilation Target)
- RCT the efficient just-in-time (JIT) compilation and ahead-of-time (AOT) compilation with Java and other execution environments

Cortex M4

- Control and signal processing capabilities
- Combination of high-efficiency signal processing functionality with the low-power, low cost and ease-of-use
- Motor control, industrial automation, automotive, power management, audio

Cortex M4 from Freescale semiconductors

- Use of thin-film storage (TFS) flash technology with configurable embedded EEPROM
- 90nm flash based microcontrollers
- Enables the use of the exact amount of Enhanced EEPROM
- Achieving millions cycles of write/erase endurance

Additional Features in M4

- **http://www.arm.com/products/processors/cortex-m/cortex-m4-processor**
- **DSP**
- **Floating Point Unit**
- **WIC**
- **Signal processing algorithm development easy through an excellent ecosystem of software tools and the Cortex Microcontroller Software Interface Standard (CMSIS)**

Cortex A15 processor

- For servers and smartphones (2010)
- Four cores like A9
- All cores in the processor coherent in that the same single operating system can run across all four
- Changes to the A15 bus allow coherency to be extended outside the cluster of four cores to multiple sets of four cores

Cortex A15 processor

- Addressing range has been extended to 1Tbyte compared with 4Gbyte for the A9
- Virtualisation control completely separates the activities of multiple operating systems running on the same processor to, for example, secure banking transactions.

Summary

We learnt

- Cortex M3 Excellent integration of the peripherals/SRAM through memory protection unit.
- Three-stage pipeline with branch prediction.
- Single cycle multiply
- Two to twelve cycle signed/unsigned divide.
- Unaligned data storage programmability
- Configurable Nested Vector Interrupt Controller
- Memory Protection Unit
- JTAG/SerialWire

We learnt

- Cortex M3 Two to twelve cycle signed/unsigned divide.
- Unaligned data storage programmability
- Configurable Nested Vector Interrupt Controller
- Memory Protection Unit
- JTAG/SerialWire
- Timer and Real Time System Clock Interrupts

We learnt

- Cortex M4 DSP Signal Processing Algorithms
- Floating Point Unit
- CMSIS

We learnt

- A15 Four Cores coherent in that the same single operating system can run across all four
- Changes to the A15 bus allow coherency to be extended outside the cluster of four cores to multiple sets of four cores
- Virtualisation control completely separates the activities of multiple operating systems

End of Lesson 07 on ARM Cortex CPU and Microcontrollers