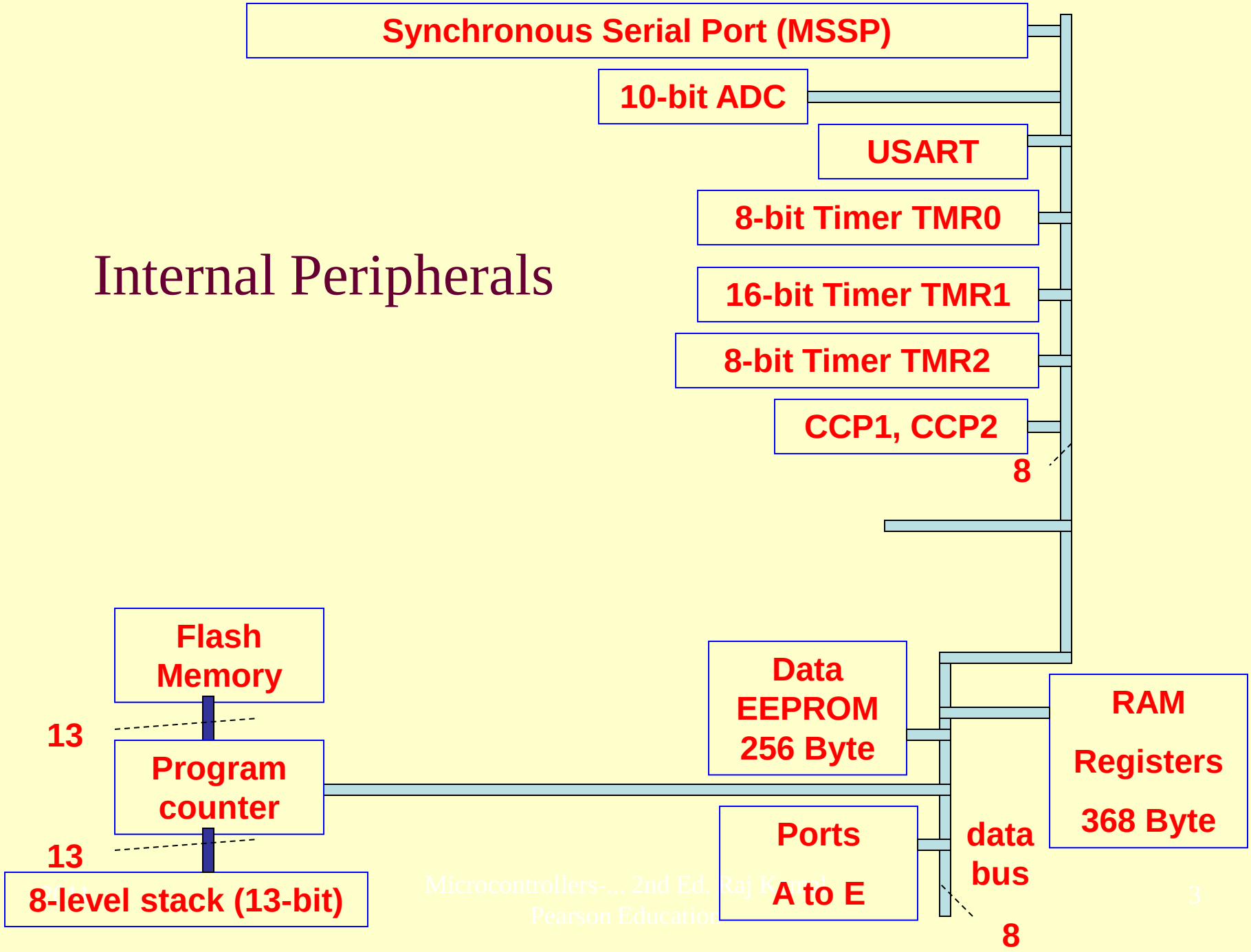
Chapter 13

PIC Family Microcontroller

Lesson 09

Timers

Internal Peripherals



Timers in PIC

- TMR0 and TMR2 2— Two 8-bit timers
- TMR1 —one 16-bit timer

TMR0 Associated Registers

- INTCON (interrupt control)
- OPTION_REG (option register)

TMR0 8-bit internal timing/counting device

- Can be loaded (written) or read
- Programmable prescaler for CLKOUT counting inputs
- CLKOUT inputs are at fOSC/4 (Oscillator frequency divided by 4)
- Each count-input after prescaling increments the counts at the timer

TMR0 8-bit internal timing/counting device

- Generates T0I (T0 overflow interrupt)
- T0IF sets on its overflow (change from 0xFF to 0x00 on increment)
- TMR0 is programmable for Internal/external clock inputs.
- Prescaler shared mutually exclusively by WDT
- The prescaler programmed using bits in OPTION_Reg (Option register)
- The prescaler is not readable/ writable

Timer TMR0

- We can select internal or external clock (through RA4 pin) for incrementing counts in the TMR0 holding register
- When using a 20 MHz crystal, the counter inputs are at the periodic intervals of 0.2 μs (200 ns) = 1 instruction cycle time
- Prescaling can be done on selecting the PS2:PS0 bits in OPTION_REG option register at address 0x81 and 0x181
- PS2-PS0 can have values 0 (000) to 7 (111)

Timer TMR0

- The prescaling factor can be set as 20 or 21, …or 27
- Prescaling can be used either by TMR0 or WDT at an instance.
- TMR0 holding register is read or written from address 0x01 or 0x101.

TMR0 SFR Readings

- At an instance is read and assume is equal to 0x7F
- Assume that it is read again after 32 periodic clock inputs of intervals of 200 ns and prescaling factor is set at 16
- The value in TMR0 0d127 + 32 ÷ 16 = 0d129 = 0x81

TMR0 SFR Readings

- After how much time, it generates the overflow interrupt and the interrupt flag will be set if at the beginning TMR0 = 0x80
- The overflow will occur after (0xFF– 0x80) increments of the TMR0.
- Then 128 × 16 × 200 ns = 57.600 μs will be time after which overflow interrupt will occur and the overflow flag will set.

16-bit Timer TMR1 Associates Registers

- TMR1L (holding register lower byte)
- TMR1H(holding register higher byte)
- INTCON (interrupt control)
- T1CON (TMR1 control)
- PIR1 (peripheral interrupt flags register1)
- PIE1 (peripheral interrupt enable register1)

TMR1 16-bit internal timing/counting device

- Can be loaded (written) or read
- The clock inputs at fOSC/4 (Oscillator frequency divided by 4)
- Programmable prescaler (1 or 2 or 4 or 8) for timer inputs to it
- Programmable for internal clock inputs /external clock inputs.
- Programmable for external clock with or without synchronisation with internal phase clocks

TMR1 16-bit internal timing/counting device

- Prescaler programmed using bits b5-b4 T1CKPS1-T1CKPS0 in T1CON
- The prescaler is not readable/writable
- Generates TMR1I (T1 overflow interrupt) and flag TMR1IF sets on its overflow (change from 0xFFFF to 0x0000 on increment)
- When CCP1 or CCP2 in compare mode can generate if configured so, a special event trigger (reset the TMR1 on that special event) at TMR1

TMR1 Holding Registers for counts

- TMR1 holding registers TMR1H-TMR1L at addresses 0x0F-0x0E
- TMR1 holding register higher and lower bytes are read or written from addresses 0x0F-0x0E

TMR1 Selecting internal clock or external for incrementing counts

- When using a 20 MHz crystal, the counter internal clock inputs are at the periodic intervals of 0.2 μs (200 ns) = 1 instruction cycle time
- Select the oscillator input for TMR1
- The oscillator built-in
- A low-power oscillator. It can oscillate up t0 200 kHz

8-bit TMR2 Associates Registers

- TMR2 (T2 holding register)
- INTCON (interrupt control)
- T2CON (TMR2 control)
- PR2 (T1 period register)
- PIR1 (peripheral interrupt flags register1)
- PIE1 (peripheral interrupt enable register1)

TMR2 8-bit internal timing/counting device

- Can be loaded (written) or read
- The clock inputs at fOSC/4 (Oscillator frequency divided by 4)
- Programmable prescaler (1 or 4 or 16) for timer inputs to it

TMR2 8-bit internal timing/counting device

- Generates TMR2I (T2 overflow interrupt)
- TMR2IF flag sets on its overflow (on change from 0xFFFF to 0x0000 on increment)
- Prescaler programmed using bits b1-b0 T2CKPS1-T2CKPS0 in T2CON
- The prescaler is not readable/writable

TMR2 8-bit internal timing/counting device

- When TMR2 increments
- When equals PR2, then it resets to 0x00 on next increment
- PR2 sets as 0xFF on PIC reset
- PR2 is readable /writable

TMR2 8-bit internal timing/counting device

- The matched output on comparison of TMR2 and PR2 is given to 4-bit post-scalar (1 or 2 or … or 15 or 16)
- Post-scaling as per bits T2OUTPS3-T2OUTPS0 b6-b5-b4-b3 in T2CON
- Post-scaling generates TMR2I (TMR2 interrupt) and sets TMR2IF flag in PIR1 bit b1

TMR2 8-bit internal timing/counting device

- TMR2 stops by resetting TMR2ON bit at T2CON b2

TMR2

- TMR2 can be used as time base for PWM mode of the CCP1, 2

Selecting internal clock for incrementing counts in the TMR2

- When using a 20 MHz crystal, the counter inputs at the periodic intervals of 0.2 μs (200 ns) = 1 instruction cycle tim
- TMR2 holding register is read or written using address 0x11
- Prescaling can be done on selecting the T2CKPS1:T2CKPS0 bits in T2CON register at address 0x12
- The bits when 00 the prescaler factor $p = 1$, when = 01 then p is 4 and when 10 or 11 the p is 16

TMR2 post scaling features

- Four TOUTPS4:TOUTPS0 bits in T2CON register can take values from 0000 to 1111 (0 to 15), then post scaling factor can be set from 1 to 16 (one plus the value of 4 bits)

TMR2 Matching with PR2

- A register PR2 at address 0x92
- When the contents of PR2 and TMR2 when becomes equal then the TMR2 interrupt flag is set on first such instance if post scaling factor $q = 1$
- TMR2 interrupt flag set on 8th such instance if $q = 8$
- The interrupt will also be generated if TMR2 interrupt is enabled

Example

- TMR*2* SFR at an instance is read and is equal to 0x7F
- Assume that it is read again after 32 periodic clock inputs of intervals of 200 ns and prescaling factor is set at 8.
- Value in TMR2 0d127 + 32 ÷ 8 = 0d131= 0x83

Example TMR2

- After how much time will it generate overflow interrupt and the interrupt flag will set if at the beginning TMR2 = 0x00
- Assuming prescaling factor is set at 4
- Assuming post scaling factor = 8
- PR2 is written 0x3F

Example TMR2

- Overflow will occur on 8th time compare and match of the TMR2 with PR2

Example TMR2

- The TMR2 increments from 0x00 to 0x3F and then increments to 0x40 in 64 × 4 × 200 ns and the TMR2 resets if post scaling factor = 1
- When post scaling factor = 8, then 8th match will occur in 64 × 4 × 200 × 8 ns. Therefore, the overflow interrupt will occur and overflow flag will set in 64 × 4 × 200 × 8 ns = 0.409600 ms.

Summary

We learnt

- 13-bit program counter
- 14-bit instructions
- ALU features
- 8-bit Data bus
- 14-bit Program code bus
- 13-bit Address bus
- 8-bit Status Register

We learnt

- TMR0 and TMR2 2— Two 8-bit timers
- TMR1 —one 16-bit timer
- Prescaling
- TMR2 Post scaling also

End of Lesson 09 on

Timers