

# Chapter 3

## 8051/8031 Family Architecture

# Lesson 06

## Serial Interface

# Synchronous SI Device

## Data Read/Write

SI data  
8-bits  
receive

**SBUF**

**SBUF**

SI data  
8-bits  
transmit

99H

99H

data in  
at P3.0

Read

Write

Data  
out at  
P3.0

clock  
in at  
P3.1

Clock  
out at  
P3.1

# SI Device Receiver mode control Bit

## Enabling Receiver of SI device

**SCON**

98H

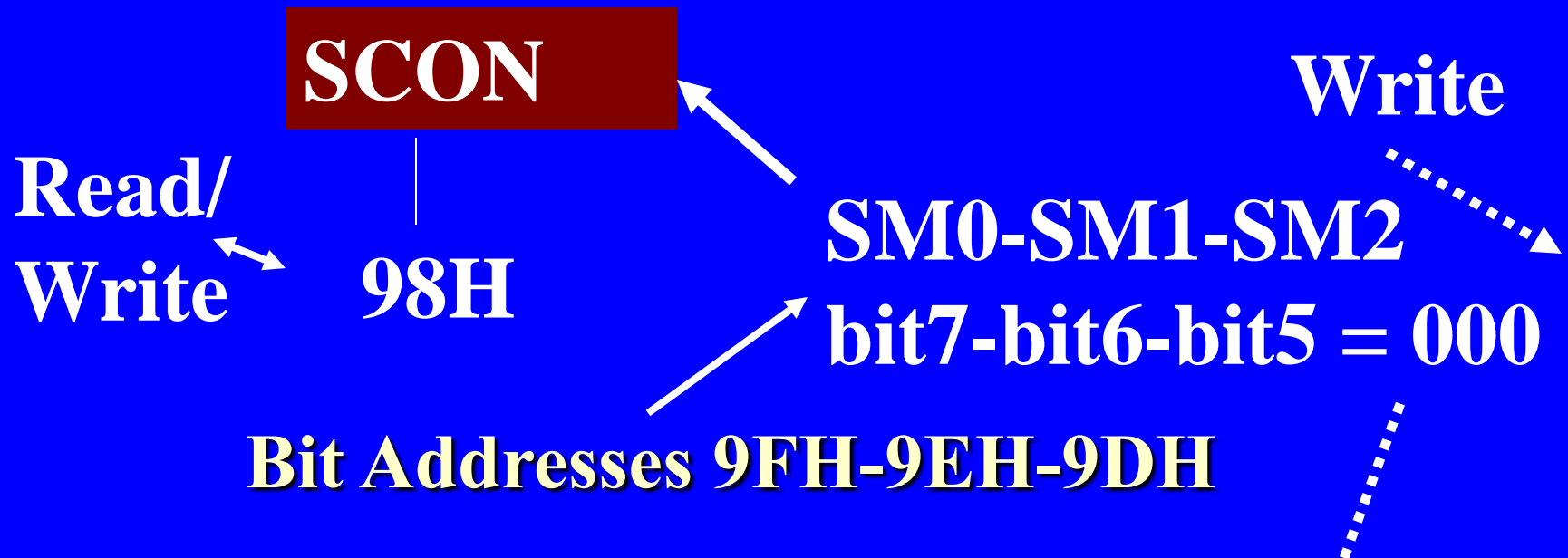
**REN**

bit4

= 1

**Bit Address 9CH**

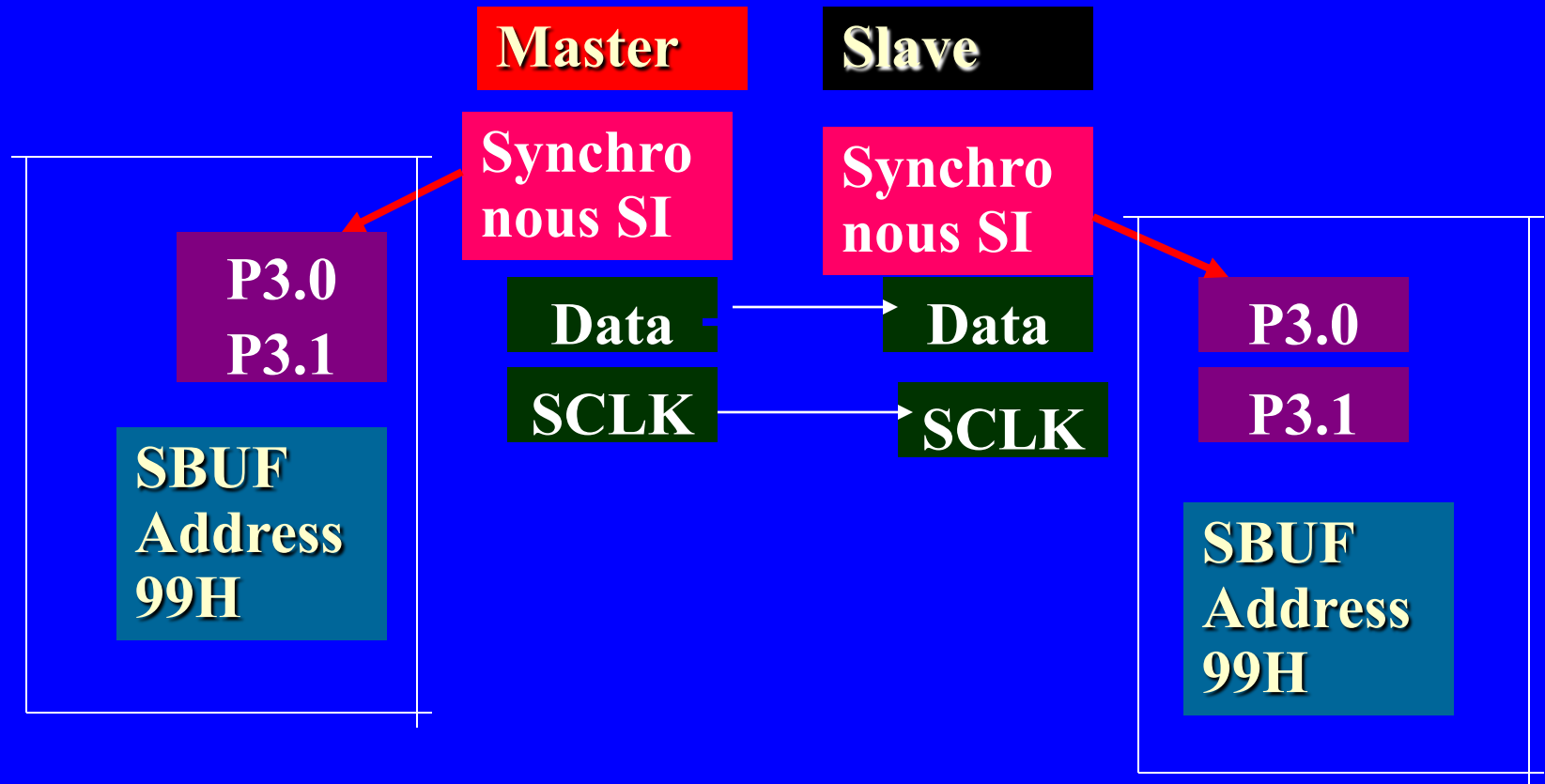
# SI Device Synchronous mode control Bits



**For Synchronous mode of SI Device**

- **Serial bit transmits at data pin and receives at slave data pin**
- **Synchronous SI devices are half duplex connected between the master and slave**
- **Synchronous SI Master device simultaneously transmits serial clock pulses so that slave can synchronize the clocking inputs with the serial data bits.**

# Synchronous SI Master- Slave Connection Between Two MCUs

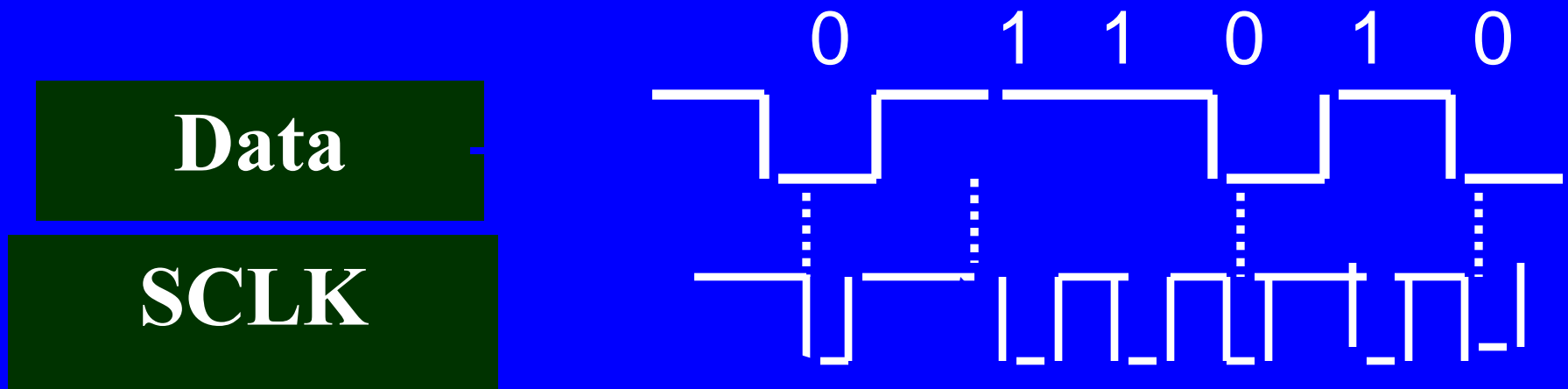


# **Synchronous SI Device Rate for SYNC Transmission**

**Serial Bit Rate 1  $\mu$ s for 12 MHz XTAL**



# Synchronous SI Master output 8 bits and 8 Clock pulses



**= 0 for  $1/12 \mu\text{s}$  and = 11/12 for  $1 \mu\text{s}$   
rate for 12Hz XTAL**

**lsb serial bit first out from SBUF**

# Synchronous SI Device Status Bits

## Synchronous SI Interrupt flags- TI and RI

**SCON**

**98H**

**Read**

**TI-RI bit1-bit0 flags  
set for Tx and Rx  
interrupts**

**TI or RI does not  
reset itself on ISR  
execution start**

**Bit Addresses 98H-9FH**

# SI UART mode

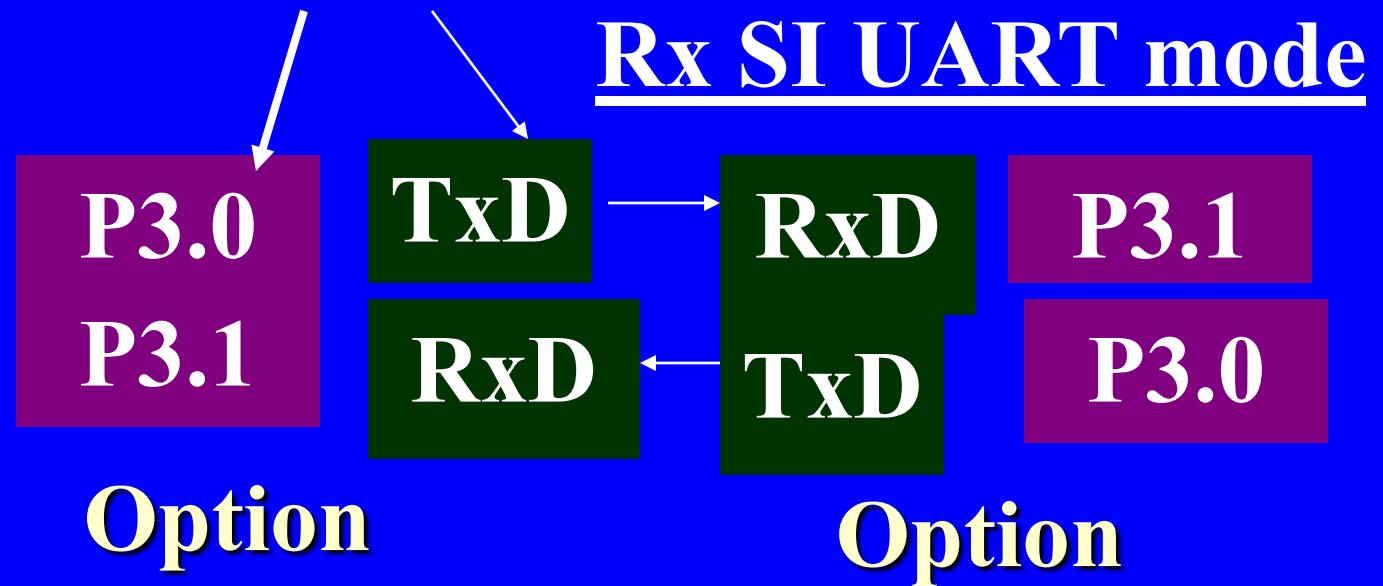
# SI UART mode

- **Serial bit SI UART mode transmits at TxD and reception at RxD pins**
- **SI UART mode devices are duplex connected between the Tx and Rx**

# SI UART mode Tx Device and Rx Device - Between the MCUs

**Tx SI UART mode**

**SBUF Address –99H**



## **SI UART mode Device Baud control by 8051 Timer**

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- **SI UART mode Tx device does not simultaneously transmit serial clock pulses. Baud is however defined same at Tx SI UART mode and Rx SI UART mode.**
- **T1 is default baud rate generator. T2 can be used in 8052**

# SI Device Receiver mode control Bit

## Enabling Receiver of SI device



# SI UART mode Device Control/status Register bits

bit7-bit6=  
01 (10Tmode1)  
10 (11Tmode2)  
11(11T mode3)

**SCON**

98H

Write/Read

Bit Addresses  
9FH-9EH-9DH  
for SM0-SM1-  
SM2

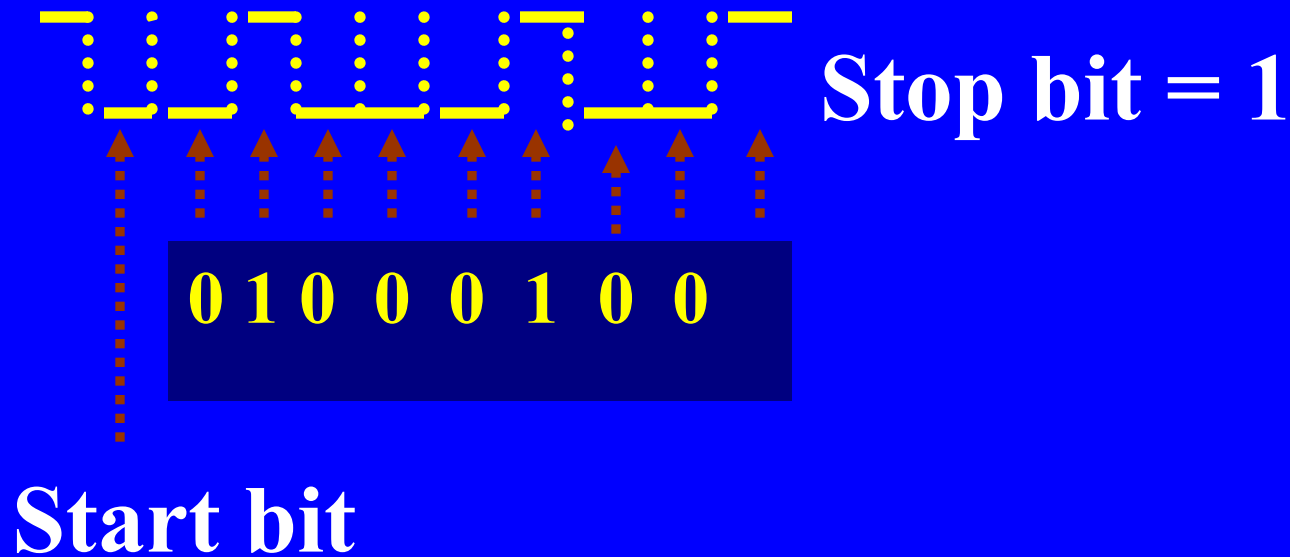
TB8 Bit  
Address- 9BH

RB8 Bit  
Address- 9AH

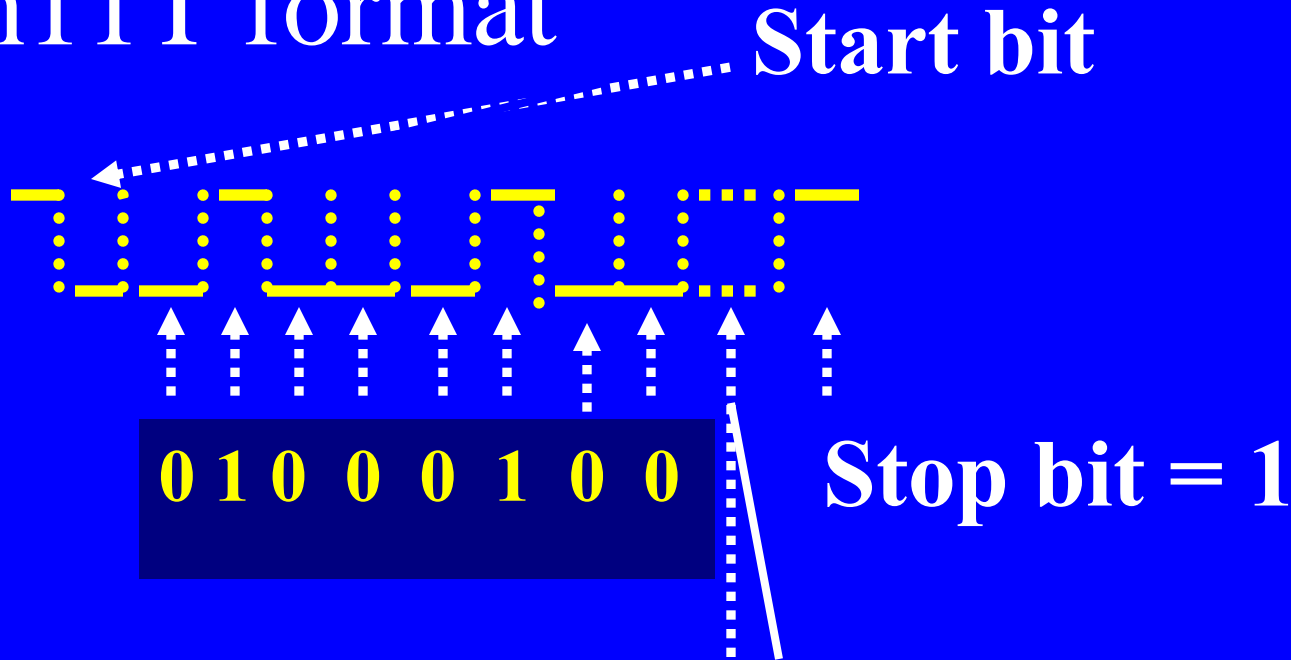
bit7-SM0 bit-6-SM1, SM2-bit 5, Send bit-3(TB8) for transmission in mode 2 and 3.  
Receives RB8 for reception in mode 2 and 3



# UART SI output 8 bits (01000100) in 10T format



UART SI output 8 bits (01000100)  
in 11T format



**TB8 = 0 or 1 as per 8th bit to  
be sent to transmitter**

# Serial Communication Control SM0-SM1 bits for modes 0, 1, 2, 3

**00 = means Synchronous mode,  
01=UART mode 1- start bit, 8 data bits, stop bit Total 10T per character )**

**10 =UART mode 2- start bit, 8 data bits, Extra TB8/Parity in 11T)**

**11=UART mode 3- start bit, 8 data bits, Extra TB8/Parity in 11T)**

**•  $T = \text{baud}^{-1}$**

# Serial Communication Control SM0-SM1 bits for modes

- Mode 1 and 3 variable baud rate by T1 periodic overflows in 8051 and T1 or T2 in 8052
- Mode 2 fixed baud rate by  $f_{osc} / 32$  or  $f_{osc} / 64$  as per PCON bytes' 7th bit, called SMOD bit.  $f_{osc} = 12 \text{ MHz}$  for 12 MHz XTAL

- $T = \text{baud}^{-1}$

# Serial Communication UART Control SM2 bit for mode 1

- When  $SM2 = 1$  and Mode is 1(10T mode) then RI at SCON.0 (98H bit address) does not activate and sets to 1 when stop bit is received 0, which is not valid.

- $T = \text{baud}^{-1}$

# Multi-processors communication in UART SI Modes 2 and 3 using SM2 bit at SCON

# Serial Communication UART Control SM2 bit for modes 2 and 3

- **When SM2 = 1 and Mode is 2 or 3 (11T mode) then RI at SCON.0 (98H bit address) does not activate and sets to 1 when RB8 bit is received 0.**

# Serial Communication UART Control SM2 bit application for mode 2 and 3 in multiprocessor communication

First each slave SM2 bit is set to 1. Each slaves activates RI (receiver interrupt flag) when RB8 = 1, therefore reads the 8-bits and check- does it corresponds to its predefined address?



**Then each slave SM2 bit is kept to 1 except the one, which successfully checked its address . That slave SM2 bit is forced = 0, it therefore keeps on activating RI each time whether RB8 = 0 or 1, therefore it reads the 8-bits and receives the data. Whenever it finds RB8 = 1, it again checks its address, if not found same as before, it forces SM2 again = 1.**

# Summary

# We learnt

- Synchronous SI - Mode 0
- SI UART mode - Modes 1, 2, 3, Use of SM2bit for multi processor communication