

Chapter 3

8051/8031 Family Architecture

Lesson 2

8051 Family MCUs Memory

Internal and External Memory

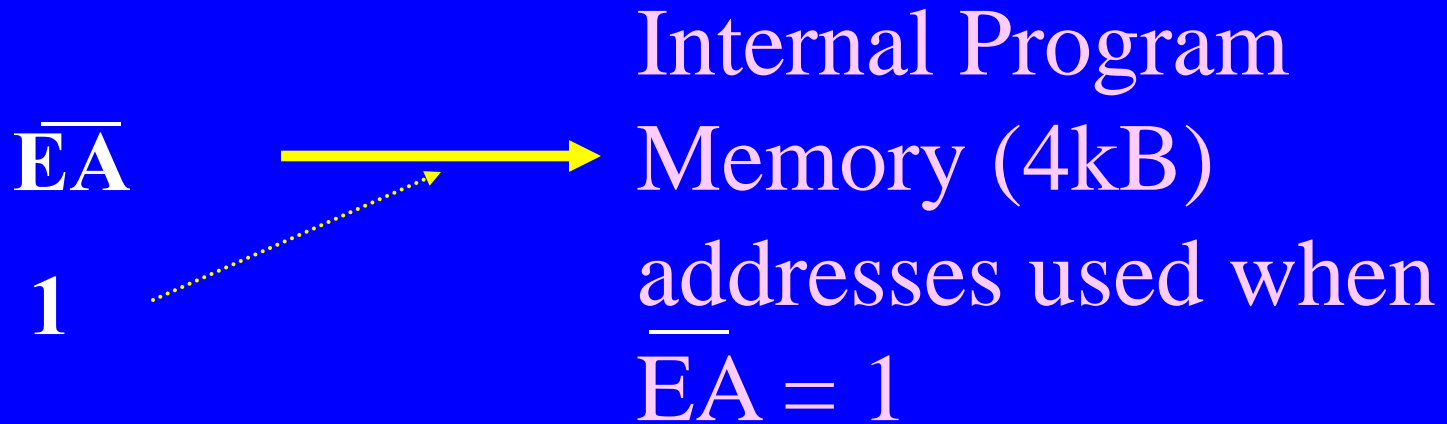
Internal memory

- 8-bit address Internal RAM Memory
- 16-bit address Internal ROM Program memory
- SFRs are separate and have 8-bit address each in separate space from internal RAM

External memory

- 16-bit address Data Memory
- 16-bit address Program memory

Internal Memory Harvard Architecture



Internal Data Memory

- 128 B 8051
- 256 B 8052

External Data Memory Architecture

8051 special feature



64 kB separate address spaces for data memory

Internal/External Program Memory Architecture

Program Memory Architecture

Address



Internal ROM

For address **0000H-0FFFH**
and $\overline{\text{EA}} = 1$ (External disable)

Address



External ROM

For address **0000H-0FFFH**
when $\overline{\text{EA}} = 0$ (External Enable)

Address



External ROM

For address **1000H-FFFFH** and
 $\overline{\text{EA}} = 0$ or **1**

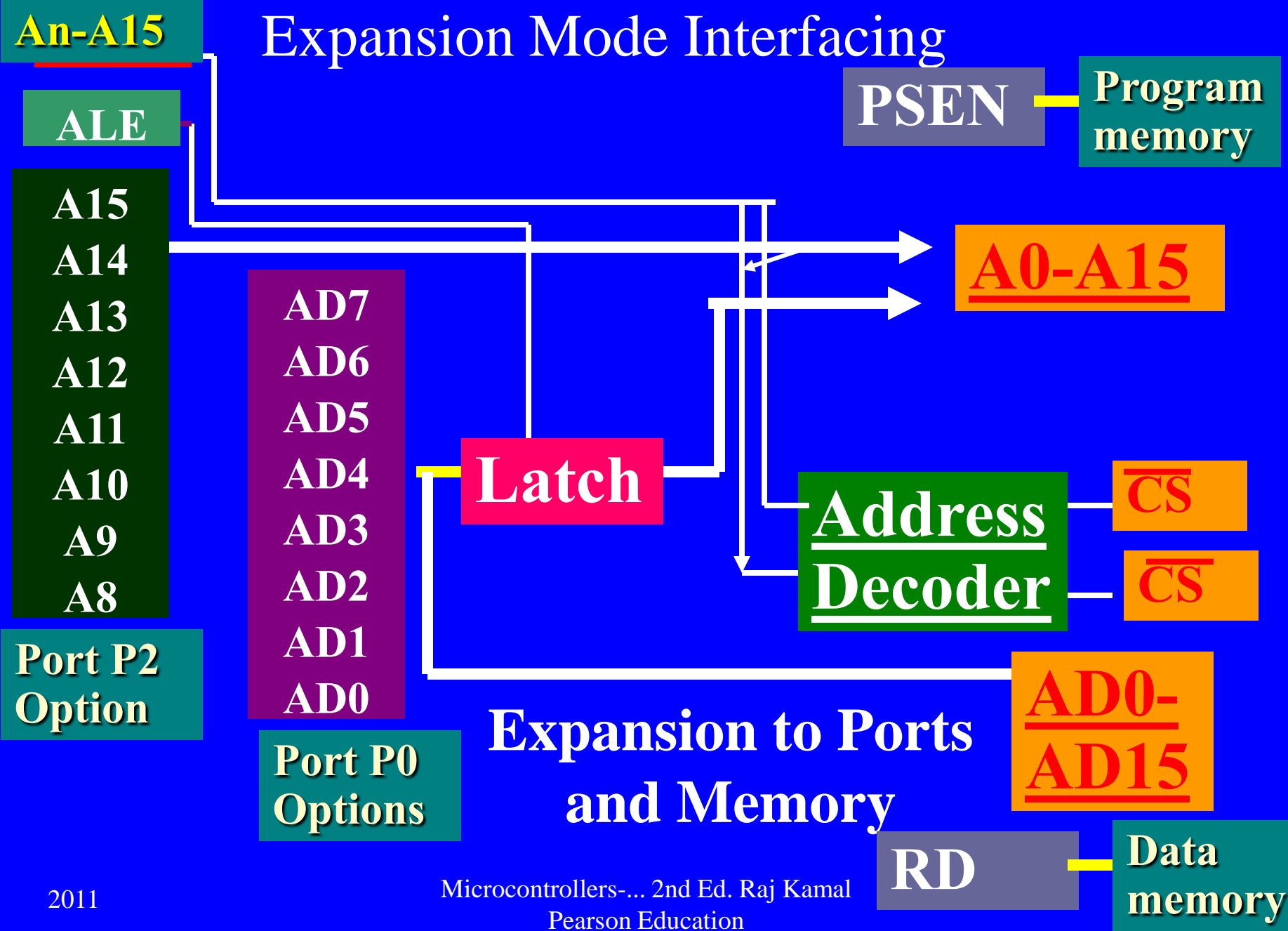
**Program,
constants
and stored
tables
Memory**

Expansion to external memory and ports

Expanded Mode used for interfacing

- External Data Memory and Ports
and
- External Program memory

Expansion Mode Interfacing



On-Chip/Off-Chip Memory Addresses

SFRs 80H-FFH

- **Used for IO and internal devices
Control and Status**
- **CPU Registers**
- **Not the part of Internal RAM**

On-Chip SFR and Memory Addresses

8051/52

Address Space

80H-FFH



**IO and internal
Devices SFRs**

System SFRs

P0,.., P3,
SBUF,
SCON,
TCON,
TMOD,
TL0,TH0,
TH1,TL1

A, B,
DPTR,
PCON,
PSW, SP,
IE, IP

Memory Access by Direct Address

80H-FFH

**IO and internal devices
Control and Status
Registers**

SP and DPTR, IP, IE, ...

00H-7FH

Internal RAM

**8-bit
addresses
00H to
FFH**

Memory Access by Indirect Address

80H-FFH

**Additional Internal
RAM 8052**

00H-7FH

Internal RAM 8051

**8-bit
addresses
00H to
FFH**

On-Chip Memory Architecture

Internal Data Memory RAM

8051

Byte Address

30H-7FH

Internal RAM 30H-7FH

20H-2FH

Internal RAM 20H-2FH

18H-1FH

Register Bank 3

10H-17H

Register Bank 2

08H-0FH

Register Bank 1

00H-07H

Register Bank 0

Each bit also addressable
Bit addresses
8-bit each 00H-7FH

Data Memory

Internal RAM as the Register Banks

Register Banks of 8 registers each

- Each Byte at the register R_i (R_0 or R_1) in a register-bank can be used as pointer to an 8-bit indirect addressing
- Each Byte at the register R_0, \dots, R_7 (R_n) can be used for a variable with 3 bits in instruction defining n and RS_0 and RS_1 at PSW defining the bank 0, 1, 2, or 3.

Off-Chip Memory Addresses

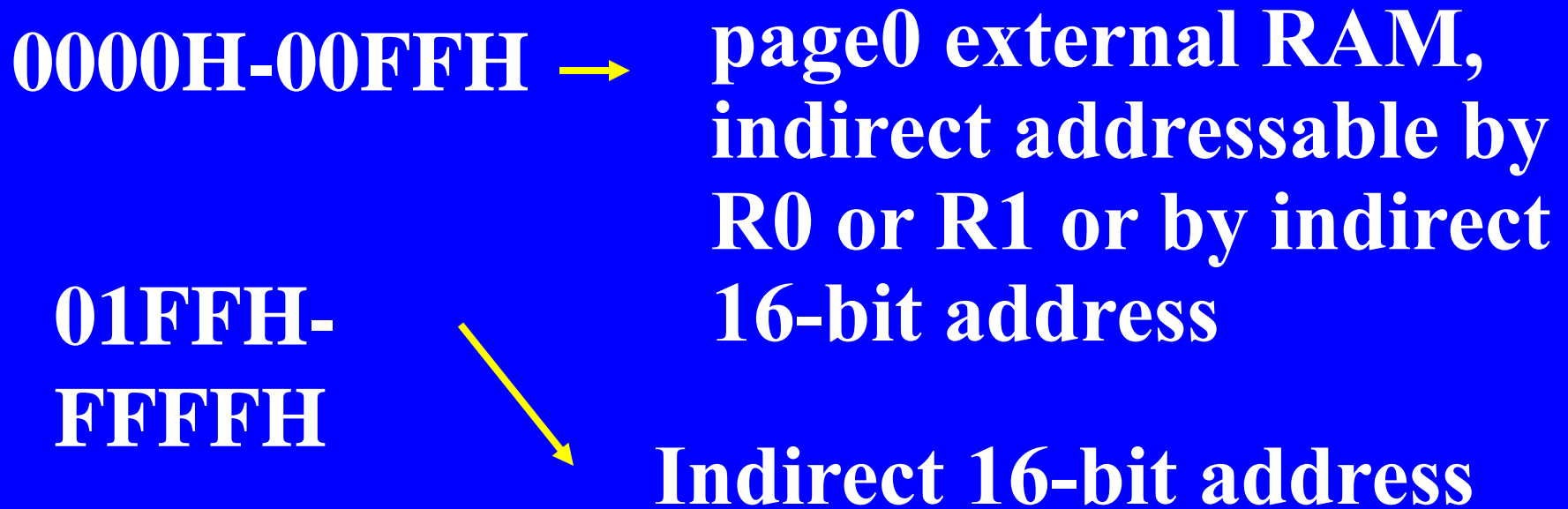
8051

**0000H-
FFFFH** **External RAM Data Memory**

**0000H-
FFFFH** **External ROM Program
Memory when $\overline{EA} = 0$**

**1000H-
FFFFH** **External ROM Program
Memory when $EA = 0$ or 1**

External RAM in 8051



Off-Chip Data Memory Architecture

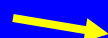
Program Memory Architecture

0000H-0002H



**Initial 3-byte
instruction for branch**

0003H-



**ISRs of maximum 8 bytes
each**

0032H,

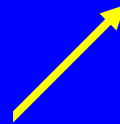
0053H-

005BH

**User Program, constants,
stored tables**

005CH-

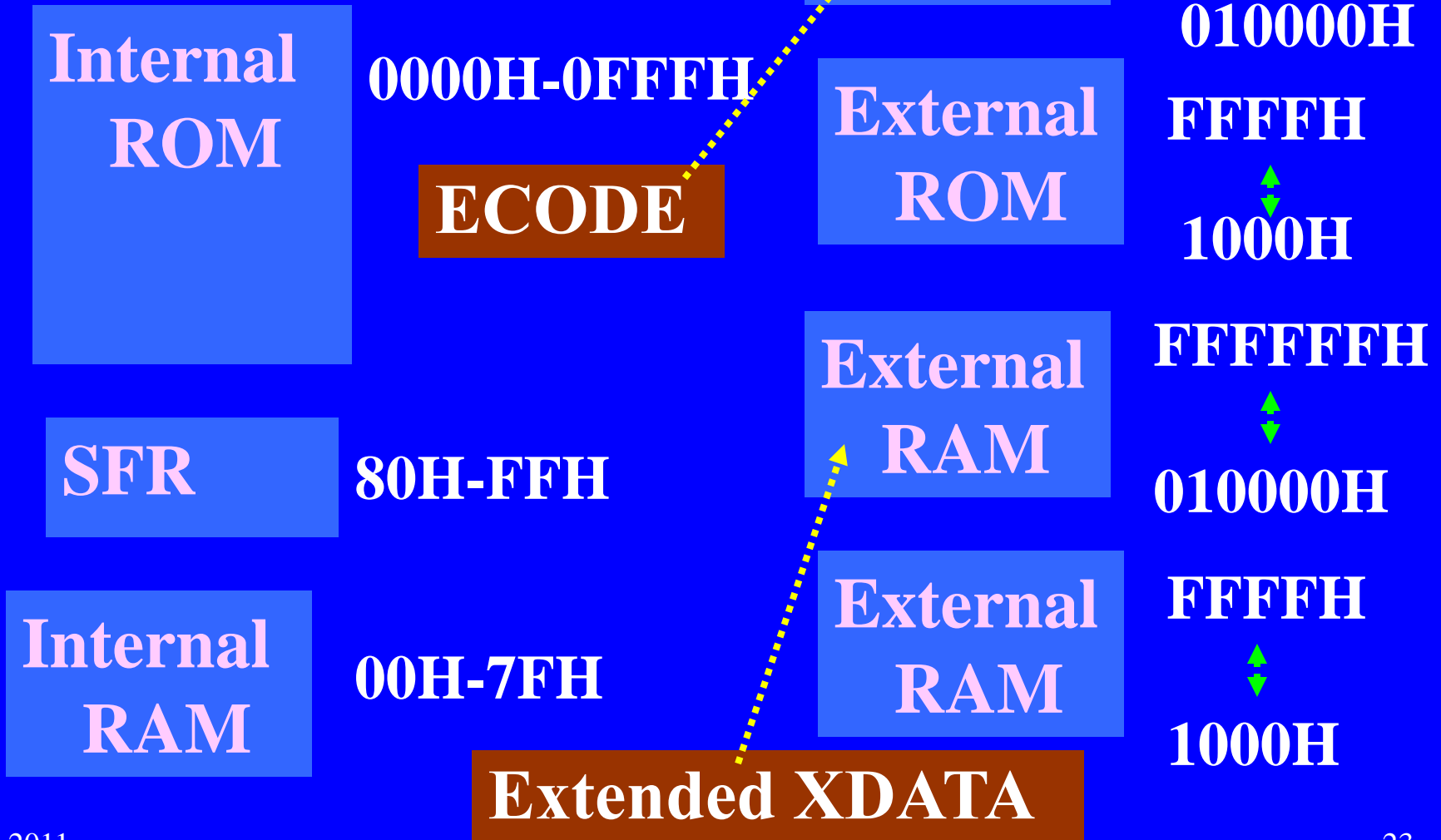
FFFFH



ROM in 8051

On-Chip/Off-Chip Memory Addresses in extended 8051

Extended 8051



Philips 8051MX

Unified Internal
and External
Addresses
Princeton
Architecture

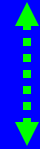


ROM



RAM

FFFFFFFH



810000H

80FFFFH



800000H

7FFFFFFH



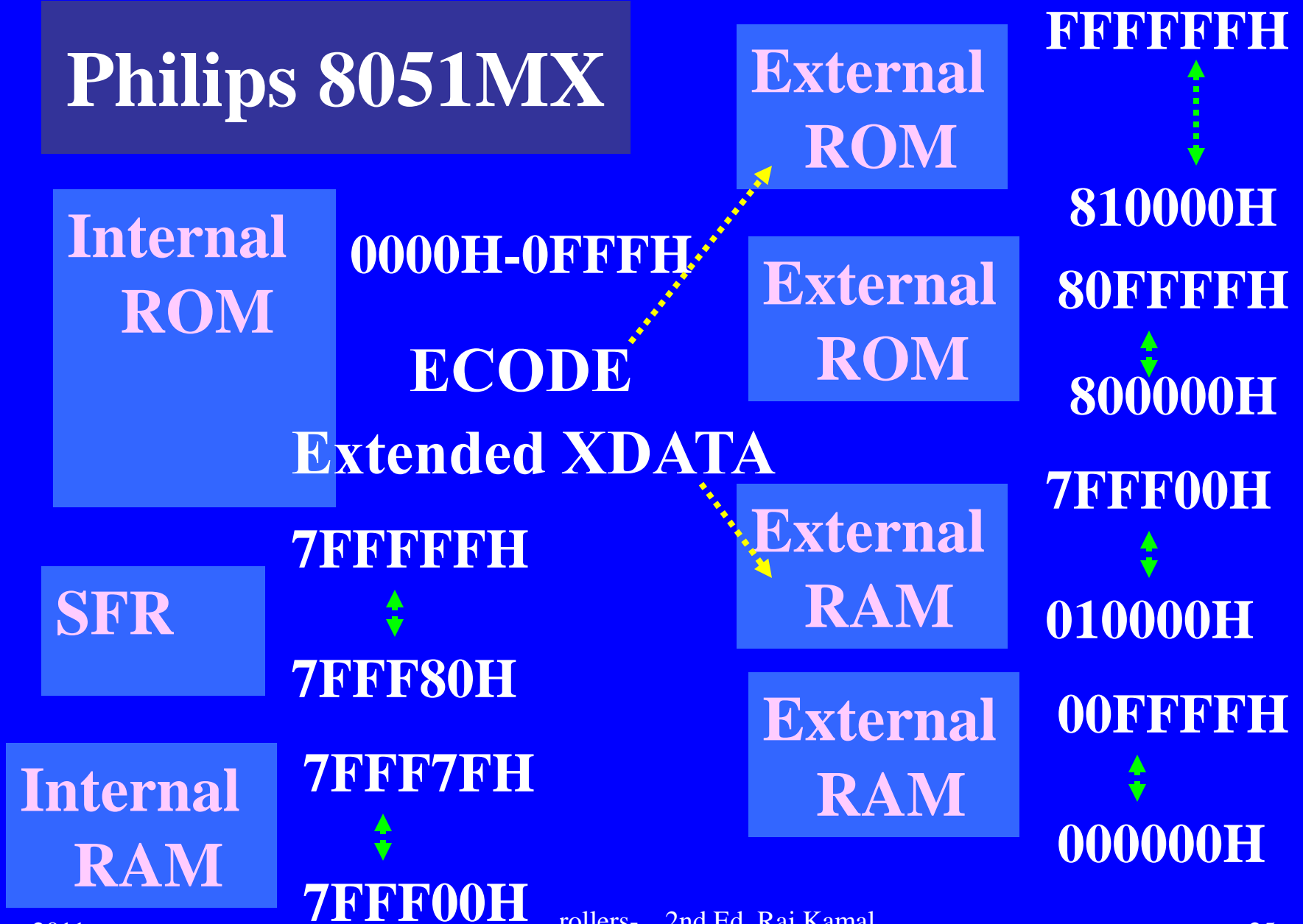
010000H

00FFFFH



000000H

Philips 8051MX



Summary

We learnt

SFRs and memory

- SFRs
- Internal RAM with bit addressable RAM and four register banks
- External RAM - Harvard Architecture
- Internal Program Memory - Harvard Architecture
- External Program Memory - Harvard Architecture

We learnt

memory

- Extended Memory in Extended 8051 version
- Unified Memory space in 8051MX