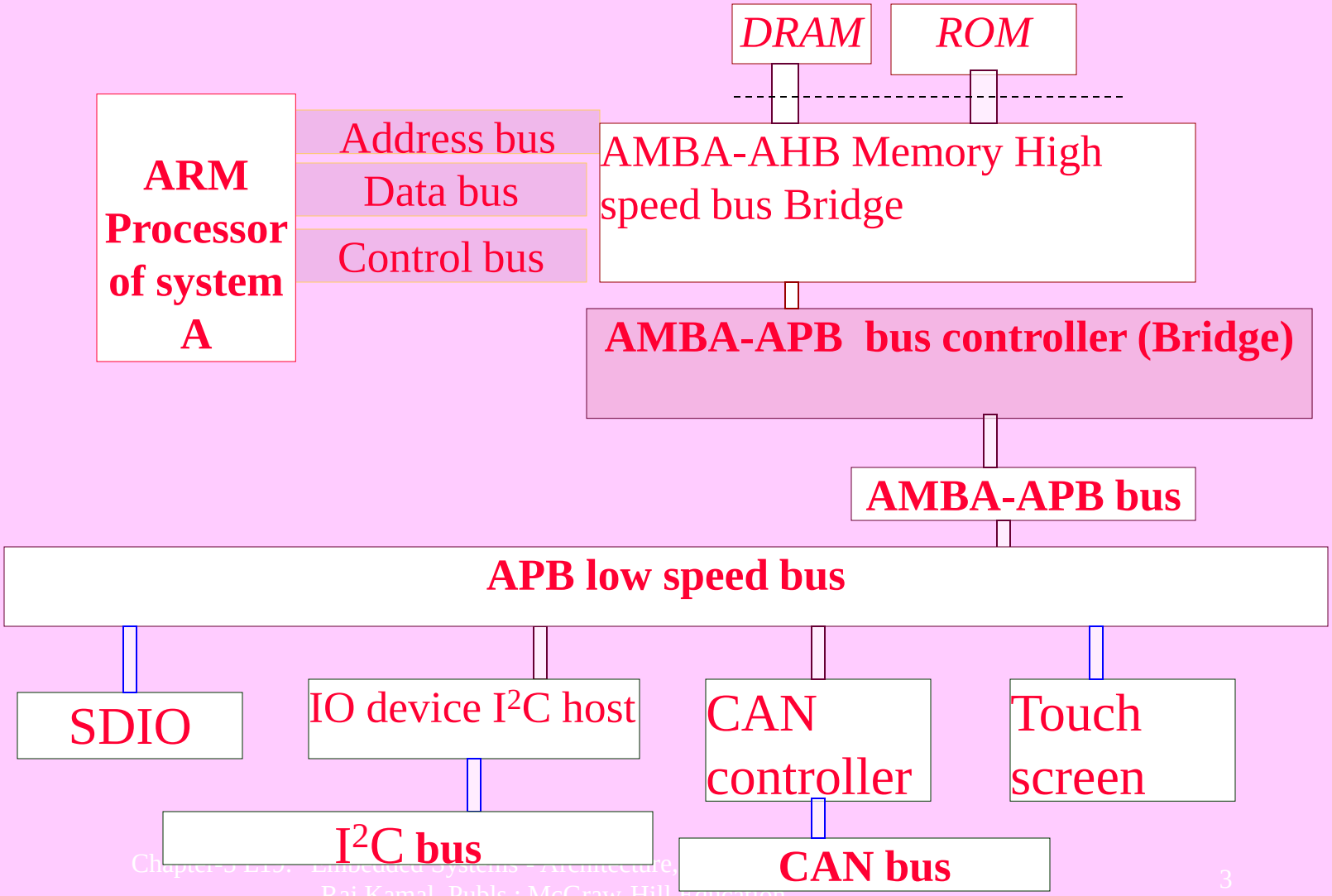
DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK–

Lesson-19: PARALLEL BUS DEVICE PROTOCOL – ARM BUS

AMBA (ARM Main Memory Bus Architecture) AHB (ARM High Performance Bus)

- AMBA-AHB interfaces the memory, external DRAM (dynamic RAM controller and on-chip I/O devices
- AMBA-AHB connects to 32-bit data and 32-bit address lines at high speed
- AHB maximum bps bandwidth─ sixteen times ARM processor clock

ARM Buses


DRAM
ROM
ARM Processor of system A
Address bus
Data bus
Control bus
AMBA-AHB Memory High speed bus Bridge
AMBA-APB bus controller (Bridge)
AMBA-APB bus
APB low speed bus
SDIO
IO device I2C host
CAN controller
Touch screen
I2C bus
CAN bus

AMBA (ARM Main Memory Bus Architecture) APB (ARM Peripheral Bus)

- AMBA -APB interfaces ARM processor with the memory AMBA-AHB and external -chip I/O devices, which operate at low speed using a bridge (AMBA-APB bridge)

AMBA-APB bridge

- Switches ARM CPU communication with the AMBA bus to APB bus.

AMBA-APB bridge

- ARM processor based microcontroller a single data bus in AMBA-AHB
- Connects to a bridge
- Integrate the bridge onto the same integrated circuit as the processor to reduce the number of chips required to build a system and thus the system cost.

AMBA-APB bridge

- The bridge communicates with the memory through a AMBA-AHB, a dedicated set of wires that transfer data between these two systems.
- A separate APB I/O bus connects the bridge to the I/O devices.

APB bus

connects

- I^2C
- touch screen
- SDIO
- MMC (multimedia card)
- USB
- CAN bus and other required interfaces to an ARM microcontroller

Summary

We learnt

- ARM bus two types – AMBA-AHB and AMBA-APB.
- AHB connects high speed memory
- APB connects the external peripherals to system memory bus through a bridge

End of Lesson 19 of Chapter 5
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Parallel Bus device Protocol- ARM Bus