# ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION – Lesson-4: SHARC, TigerSHARC and DSPs

# 1. SHARC

# SHARC

- Processor from Analog Devices.
- SHARC stands for Super Harvard Single-Chip Computer
- Super Harvard architecture means more than one set of address and data buses for data
- For example, set J of address and data buses for data-memory space, set K of address and data buses for data-memory space, and set I of address and data buses for program-memory space

# SHARC functions

- Program memory configurable as program and data memory parts (Princeton architecture)
- SHARC functions as VLIW (very large instruction word) processor.
- used in large number of DSP applications.
- Controlled power dissipation in floating point ALU.
- Different SHARCs can link by serial communication between them

# SHARC features

- ON chip memory 1 MB Program memory and data memory (Harvard architecture)
- External OFF chip memory
- OFF chip as well as ON-chip Memory can be confirgured for 32-bit or 48 bit words.

# Integer operation features

- Integer and saturation integer arithmetic both
- Saturation integer example─ integer after operation should limit to a maximum value ─ required in graphic processing

# Parallel Processing features

- Supports processing instruction level parallelism as well as memory access parallelism.
- Multiple data accesses in a single instruction

# Addressing Features

- SHARC 32-bit address space for accesses
- Accesses 16 GB or 20 GB or 24 GB as per the word size ( 32-bit, 40-bit or 48 bit) configured in the memory for each address.
- When word size = 32-bit then external memory configuration addressable space is 16 GB ($2^{32} \times 4$) bytes

# Word size features

- Provides for two word sizes 32-bit and 48-bit.
- SHARC two full sets of 16 general-purpose registers, therfore fast context switching
- Allows multtasking OS and multithreading.
- Registers are called R0 to R15 or F0 o F15 depneding upon integer operation configuration or floating point configuration.
- Registers are of 32-bit. A few registers are special, of 48 bits that may also be accesses as pair of 16-bit and 32-bit registers.

# SHARC features

- instruction word 48-bits
- 32-bit data word for integer and floating point operations and
- 40-bit extended floating point.
- Smaller 16 or 8 bit must also store as full 32-bit data. Therefore, the big endian or little endian data alignment is not considered during processing with carry also extended for rotating (*RRX*).

# 2. TigerSHARC

# TigerSHARC

- Highest performance density family of processors from Analog Devices
- Precision high-performance integrated circuits used in analog and digital signal processing applications
- designed for multiprocessing applications and for peak performance greater than BFLOPS (billion floating-point operations per second)

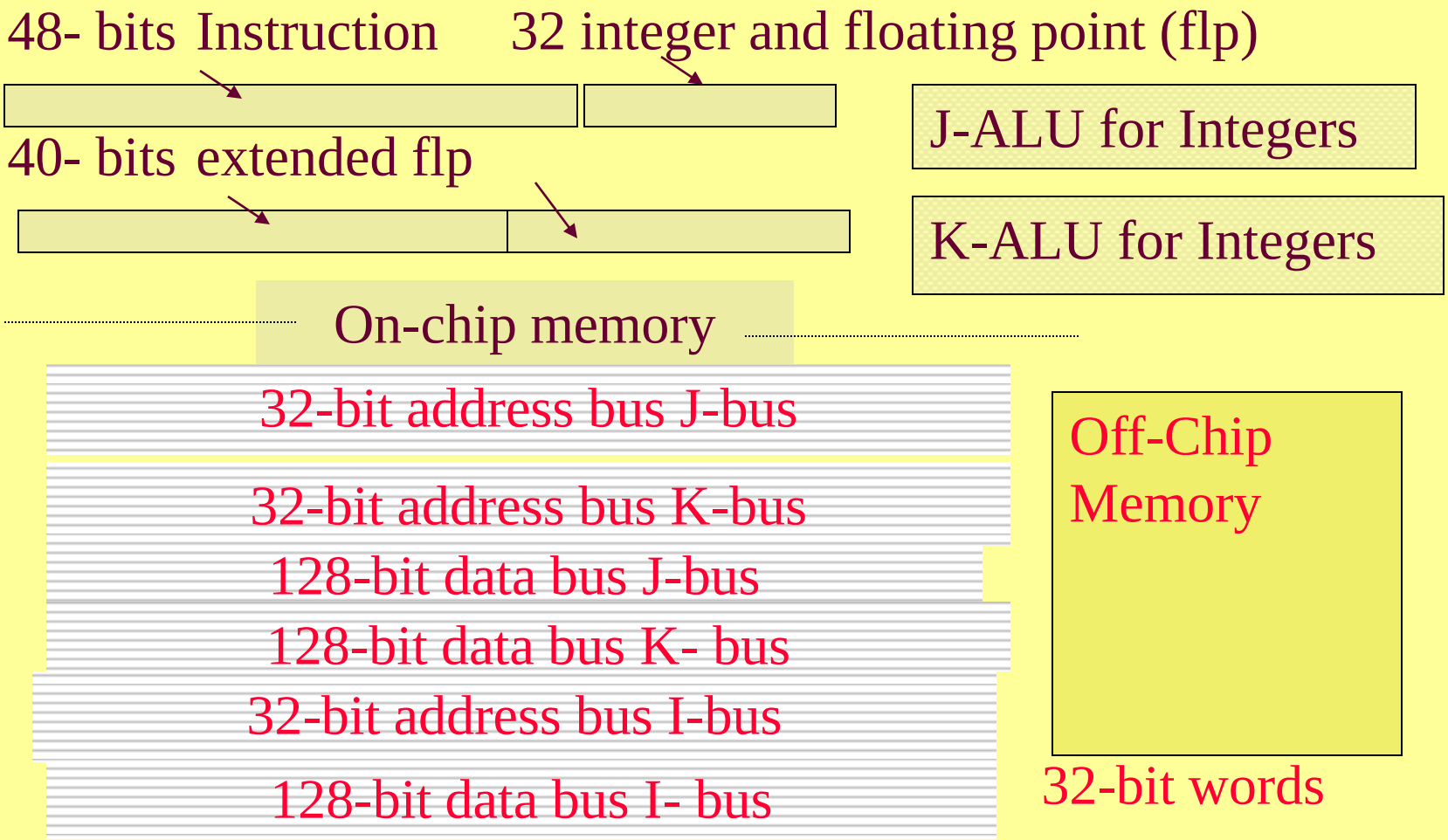
# Example

- ADSP-TS203SABP-050 processor processes using 250 MHz clock and on chip memory of 6 M bits and operates at 1.2V/3.3 V
- Low voltage design helps in processing with little power dissipation.
- Analog Devices claims the highest performance per Watt.

# TigerSHARC

- MultipleTigerSHARCs can connect by serial communication at 1 GBps.
- A TigerSHARC version has 24 M bits ON-chip memory.
- Two ALUs and twos set of address and data buses for data memory
- On set of address and data buses for program memory
- TigerSHARC is available as IP core also so that new applications and enhancements can be developed.

# TigerSHARC super Harvard architecture and registers in ADSP-TS203S



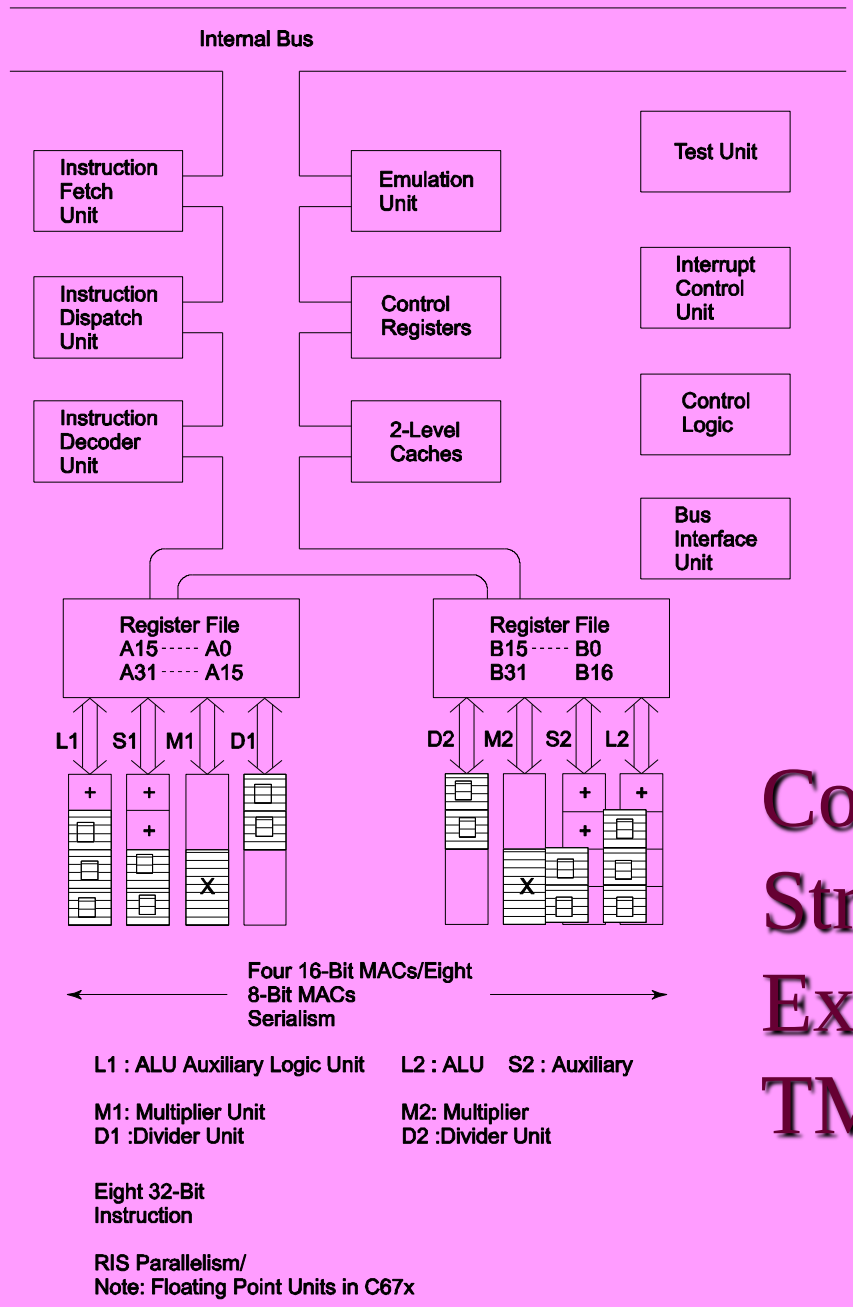
# 3. DSPs

# DSP

- Advanced signal processor circuits
- MAC (Multiply and Accumulate) unit (s)─ provides fast multiplication of two operands and accumulating results at a single address.
- MAC unit computes fast an expression such as the following summation. $y_n = \Sigma(a_i \times x_{n-i})$ where the sum is made for $i = 0, 1, 2, \ldots, N\text{-}1$. Here $i$, $n$ and $N$ are the integers, $a_i$ is a coefficient, $x_j$ is independent variable or an input element and $y_k$ is the dependent variable or an output element.

# DSP

- DSP processors invariably have Harvard architecture.
- Caches are organized in Harvard architecture (separate I-cache and D-Cache
- Basic Units: MDR, Internal Bus, Data bus, Address bus, control bus, Bus Interface Unit, Instruction fetch register, Instruction decoder, Control unit, Instruction Cache, Data Cache, multistage pipeline processing, multi-line superscalar processing for obtaining processing speed higher than one instruction per clock cycle, Program counter




# Core and Special Structure units in an Exemplary DSP, TMS320C64x DSP

# DSP special structural units

- Packed Data processing
- Parallel Execution MAC units
- Special Instructions
- Instruction Packing unit

# Parallel Processing features

- Supports processing instruction level parallelism as well as memory access parallelism.
- Multiple data accesses in a single instruction

# Summary

We learnt

- SHARC has super Harvard architecture
- 32-bit address buses and 128-bit data buses in three sets J, K and I.
- TigerSHARC
- Peak performance greater than BFLOPS
- Low voltage design helps in processing with little power dissipation,
- Claims the highest performance per Watt

# Summary

We learnt

- DSP for digital signal processing
- Harvard architecture
- MAC (Multiply and Accumulate) unit
- VLIW (instruction packaging unit)
- TMS320C64x

# End of Lesson 4 of Chapter 4
# on
# SHARC, TigerSHARC and DSPs