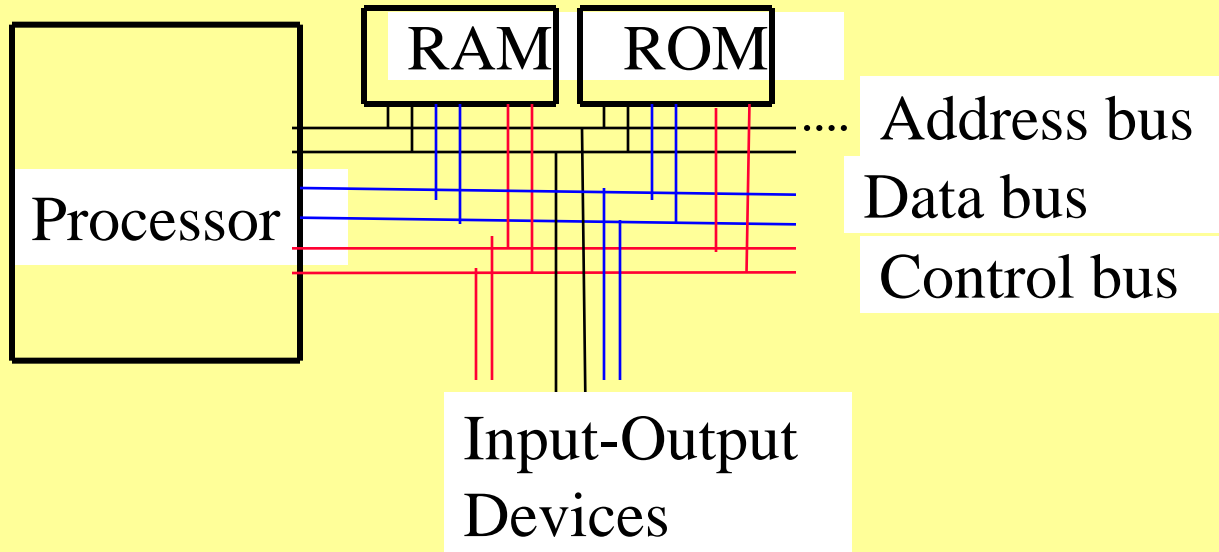


# ADVANCED PROCESSOR ARCHITECTURES AND MEMORY ORGANISATION –

## Lesson-1: Processor organisation and Instruction Level Parallism

# 1. Processor Organisation

# Processor, Memory and buses



# Processor

- *ALU*
- Processor circuit does sequential operations and a *clock* guides these.
- *Program counter* and *stack pointer*, which points to the instruction to be fetched and top of the data pushed into the stack.
- Certain processor have on-chip memory management unit (MMU)

# Registers

- General-purpose registers.
- Registers organize onto a common internal bus of the processor. A register is of 32, 16 or 8 bits depending on whether the ALU performs at an instance a 32- or 16- or 8-bit operation

# CISC

- Processor may have CISC (Complex Instruction Set Computer) or RISC (Reduced Instruction Set Computer) architecture may affect the system design.
- *CISC* has ability to process complex instructions and complex data sets with fewer registers as it provides for a large number of addressing modes.

# RISC

- Simpler instructions and all in a single cycle per instruction.
- New RISC processors, such as ARM 7 and ARM9 also provide for a few most useful CISC instructions also.
- *CISC converges to a RISC implementation* because the most instructions are hardwired and implement in single clock cycle

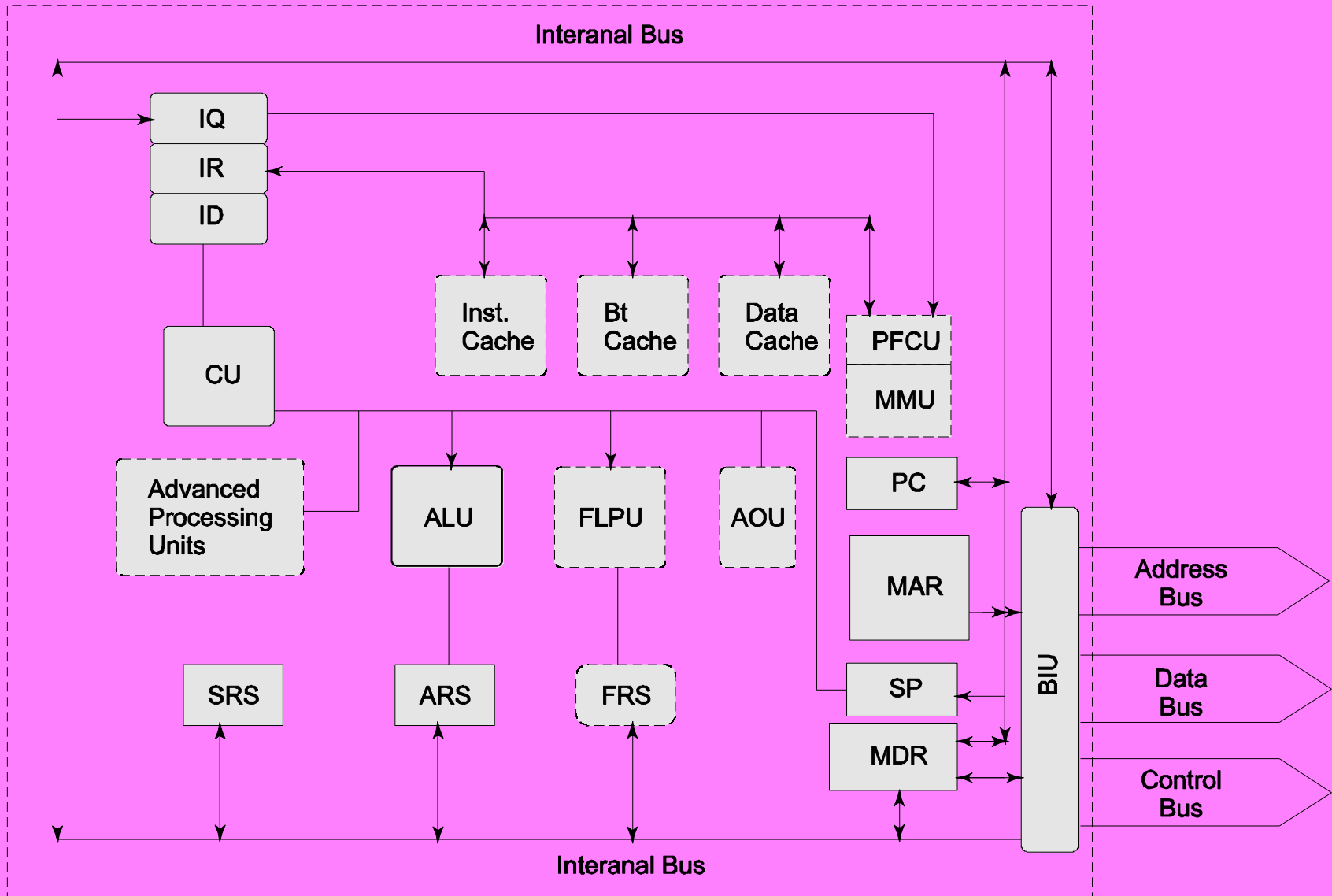
# Interrupts

- Processor provides for the inputs for *external interrupts* so that the external circuits can send the interrupt signals
- May possess an *internal interrupt controller* (handler) to program the service routine priorities and to allocate vector addresses.



## **2 The Structural Units in a Processor:**

# Organisation of various structural units of processor



# Buses

- 1) Internal and external buses interconnect the processor internal units with the external system memories, I/O devices and all other system elements
- 2) Address, data and control buses

# MDR, MAR, BIU , PC and SP

- 3) MDR (memory data register) holds tMDR, MAR, BIU, PC and SP A andhe accessed byte or word
- 4) MAR (memory address register) holds the address
- 5) BIU (Bus Interface Unit)
- 6) Program Counter or Instruction Pointer and
- 7) Stack Pointer

# Registers

- 8) ARS (Application Register Set): Set of on-chip registers for use in the application program. Register set — also called file and associates an ALU or FLPU.
- 9) Register window- a subset of registers with each subset storing static variables and status words of a task or program thread. Changing windows help in fast context-switching in a program.

# ALU, FLPU

10) ALU and FLPU (Arithmetic and Logic operations Unit and Floating Points operations Unit). FLPU associates a FLP register set for operations.

# Caches

12) Instruction, Data and Branch Target Caches and associated PFCU (Prefetch control unit) for pre-fetching the instructions, data and next branch target instructions, respectively.

Multi-way Cache – Example- 16 kB, 32-way Instruction cache with 32 byte block for data and 16 kB in ARM

Cache block – Enables simultaneous caching of several memory locations of a set of instructions

# AOU

13) AOU (Atomic Operations Unit ) An instruction is broken into number of processor-instructions called atomic operations (AOs), AOU finishes the AOs before an interrupt of the process occurs - Prevents problems arising out of incomplete processor-operations on the shared data in the programs



## Features in most processors

- Fixed Instruction Cycle Time — RISC processor core
- 32-bit Internal Bus Width— to facilitate the availability of arithmetic operations on 32-bit operands in a single cycle. The 32-bit bus — a necessity for signal processing and control system instructions.

## Features in most processor

- Program-Counter (PC) bits and its reset value
- Stack-Pointer bits with and its initial reset value

## Features in advanced architectures

- Instruction, Branch Target and Data Cache
- Memory-Management unit (MMU)
- Floating Point Processing unit
- System Register Set

## Features in advanced architectures

- Floating Point Register Set
- Pre-fetch Control Unit for data into the I- and D-caches
- Instruction level parallelism units (i) multistage pipeline (ii) Multi-line superscalar processing

## RISC architecture

- Executing most instructions on in a single clock cycle execution per instruction (by hardwired implementation of instructions)
- Using multiple register-sets or register-windows or files and
- Greatly reducing ALU dependency on the external memory accesses for data due to the reduced number of addressing modes provided for the ALU instructions.

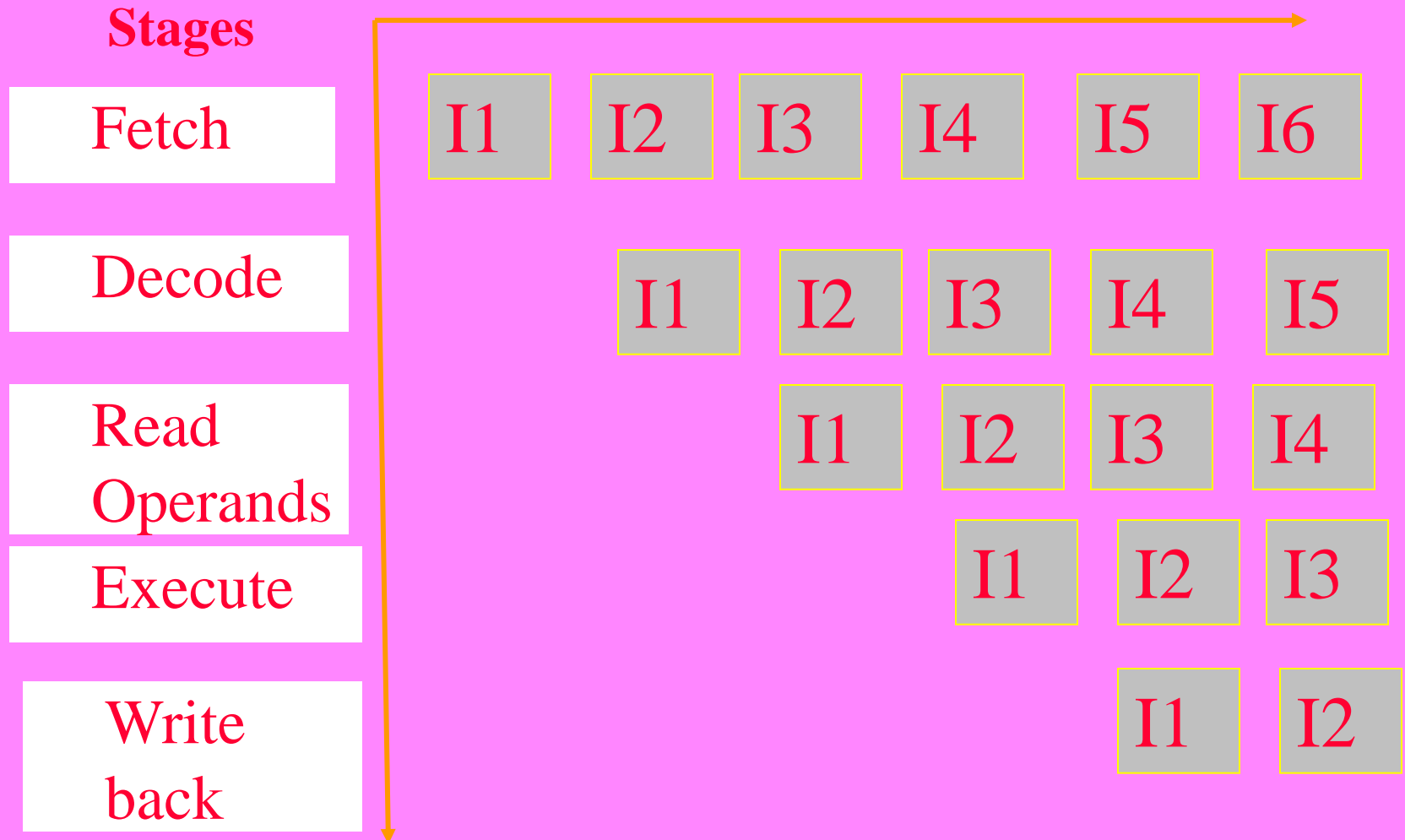
# RISC Load and store architecture

- Before ALU operations, the operands are loaded into the registers and similarly the write back result is in the register and then stored at the external memory addresses

# 3. INSTRUCTION LEVEL PARALLELISM

# 5- stage pipeline

Successive Clock Intervals





# Cycles

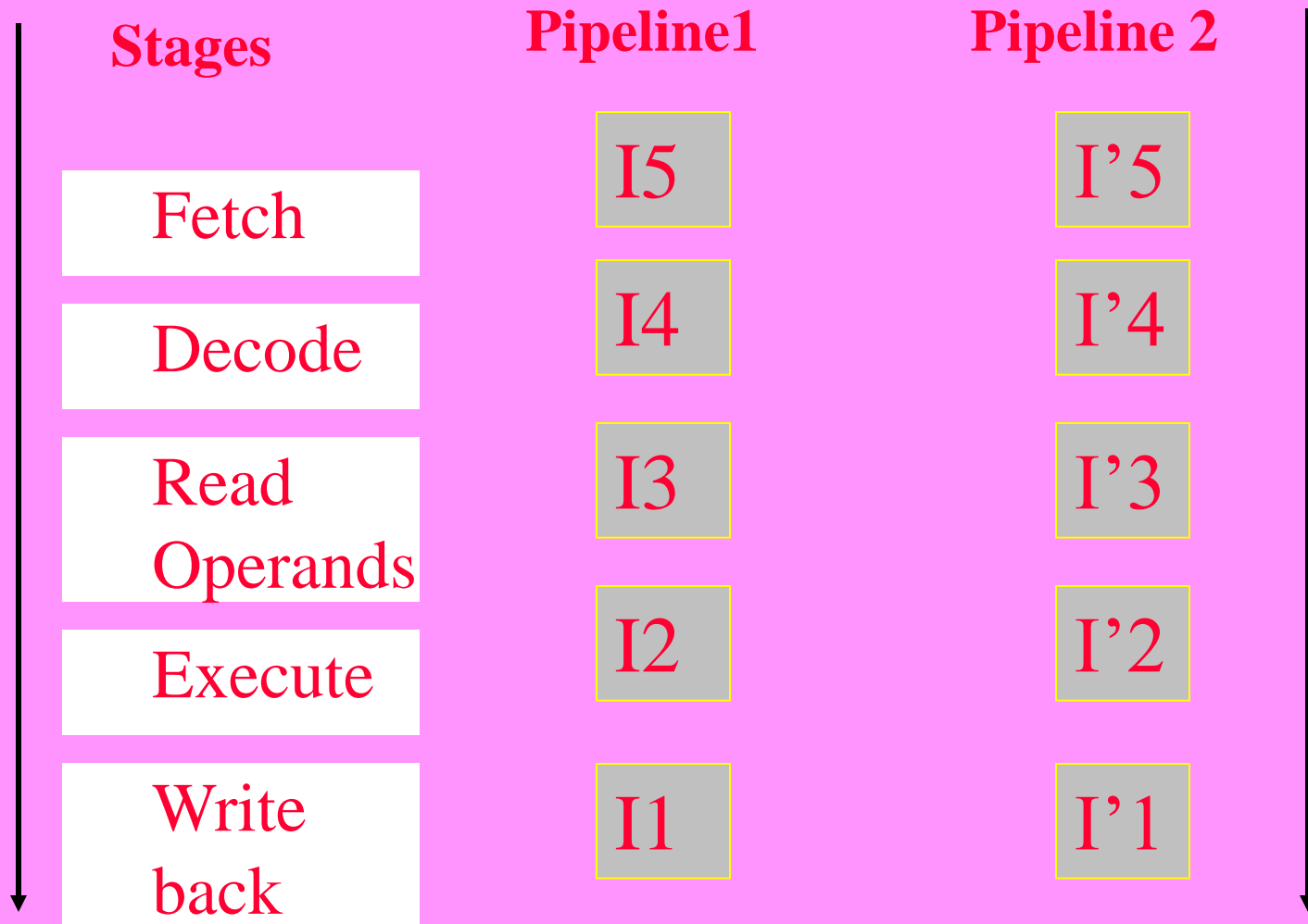
- On cycle 1, the first instruction *I0* enters the instruction fetch (IF) stage of the pipeline and stops at pipeline latch (buffer) between instruction fetch and instruction decode (ID) stage of the pipeline.
- On cycle 2, the second instruction *I1* enters the instruction fetch stage, while instruction *I0* proceeds to instruction decode stage.
- On cycle 3 the instruction *I2* enters the register (inputs) read (RR) stage, instruction *I1* is in the instruction decode stage, and instruction *I0* enters instruction fetch stage.

# Cycles

- Instructions proceed through the pipeline at one stage per cycle until they reach the register (result) write-back (WB) stage, at which point execution of the instruction *I0* is complete.
- On cycle 6 in the example, instructions *I1* through *I5* are in the pipeline, while instruction *I0* has completed and is no longer in the pipeline.
- The pipelined processor is still executing instructions at a rate (throughput) of one instruction per cycle, but the latency of each instruction is now 5 cycles instead of 1. But each cycle period is now 1/5 or less compared to the case without pipelining. Thus processing performance can improve or more times in five stage pipeline .

# 3. INSTRUCTION PIPELING

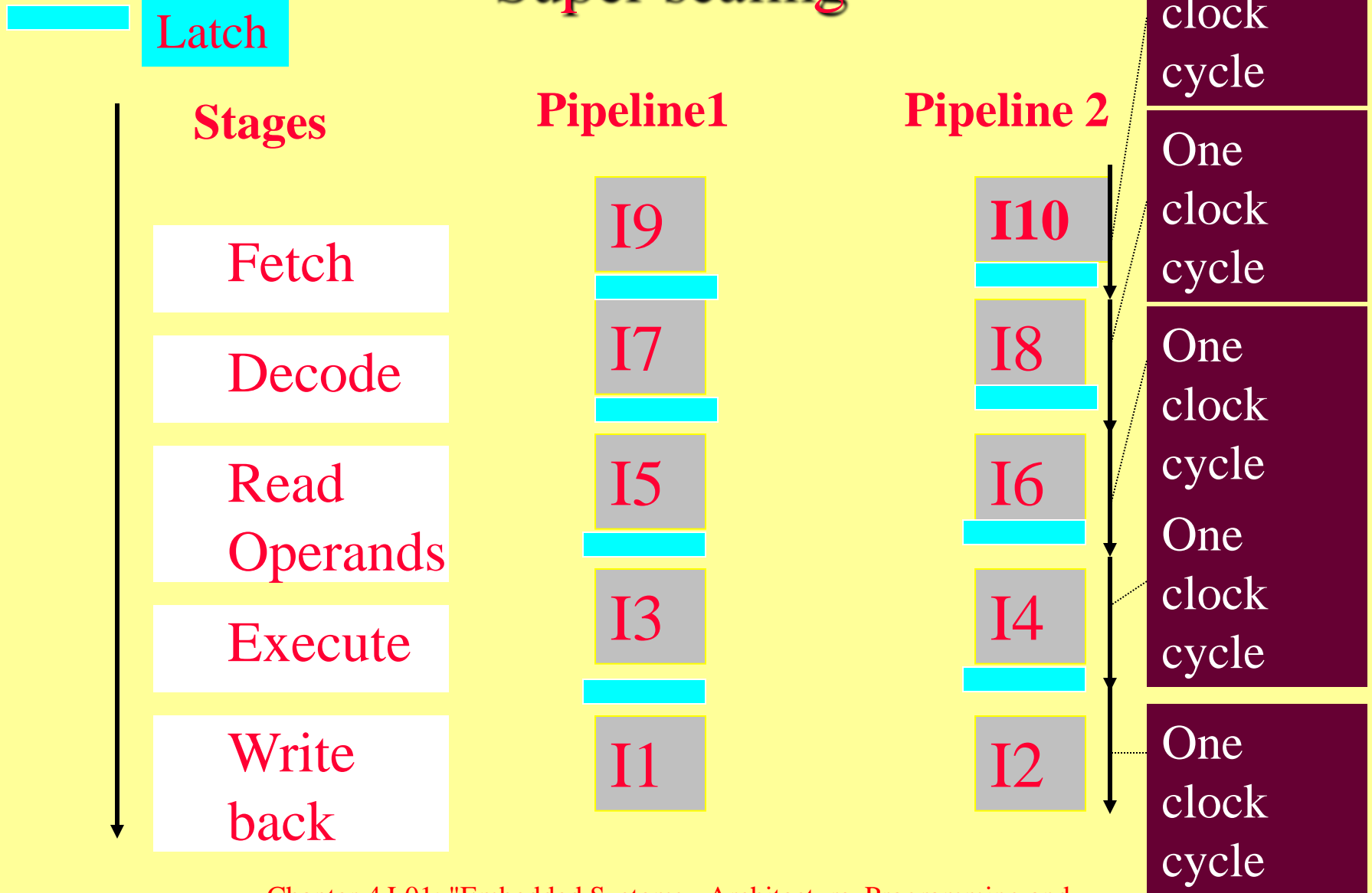
# Super scaling



# Instruction level parallelism (ILP)

- Execute several instructions is parallel. Two or more instructions execute in parallel as well as in pipeline.
- During the in which two parallel pipelines in a processor and two instructions  $I_n$  and  $I_{n+1}$  executing in parallel at the separate execution units

# Super scaling



# DMA (Direct Memory Access) Controller

- External Devices can directly write and read into the blocks of RAM using the DMA controller, when the buses are not in use of the processor

# Direct memory access (DMA) Controller

- Multiple DMA channels on chip.
- When there are number of I/O devices and an I/O device needs to access a multi byte data set fast, the system memory on-chip DMA controller help greatly



# Summary

We learnt

- Processor, address, data and control buses and Memory
- CISC and RISC

# We learnt

- Structural units in a processor
- Caches, Register set(s), buses
- RISC architecture features
- MMU, Floating Point Processing
- Instruction pipelining
- Instruction Level Parallelism

End of Lesson 1 of Chapter 4  
on  
Processor Organisation and Instruction  
Level Parallism