8051, AVR, ARM MICROCONTROLLERS AND REAL WORLD INTERFACING AND IOs USING BUSES –

Lesson-5: ATMEL AVR ® AND ARM MICROCONTROLLERS

1. ATMEL AVR® microcontroller architecture

AVR®

- Stands for **A**lf (Egil Bogen) and **V**egard (Wollan) **R**ISC processor
- RISC means reduced instruction set computer
- Provides for selected few addressing modes for addressing the operands in the arithmetic, logical and other instructions

AVR®

- Each instruction takes 1 cycle time. Instructions implement in hardware by hardwired implementation not by a micro-program unit inside the processor.]

AVR® 8

- 8-bit arithmetic logic unit (ALU)
- Internal bus width is 8-bit
- Single stage pipeline, which means one instruction fetched in advance.
- Harvard memory architecture, the program memory and data memory have separate address spaces from 0x0000 and separate control signal(s).

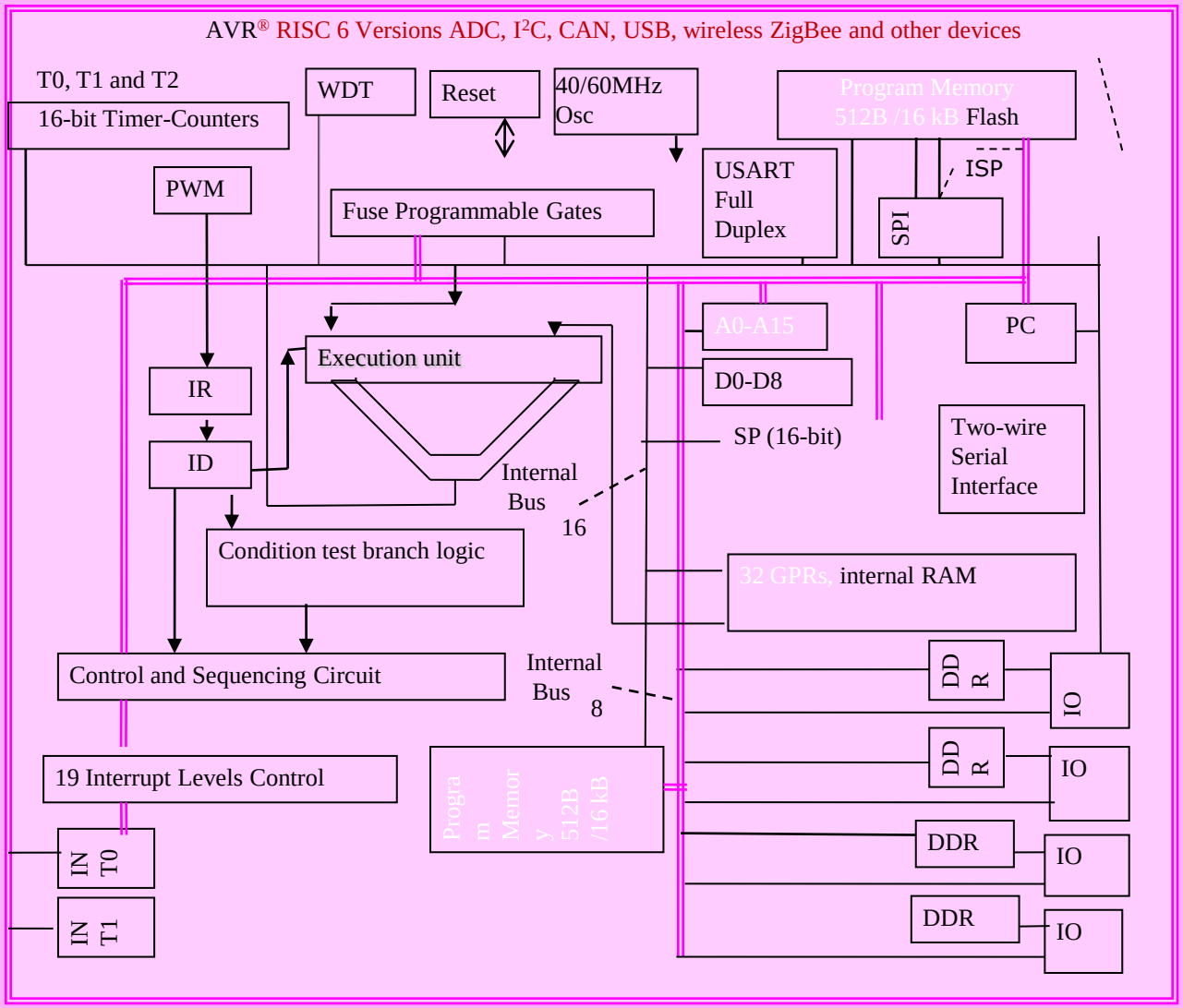
Six groups of microcontrollers

- *tiny* (512 to 16 kB program memory)
- *mega* (4 to 512 kB program memory)
- *xmega* (16 to 384 kB program memory)
- *application specific additional controller unit*s for LCD, CAN, USB, ZigBee and advanced PWM, and fuse programmable *additional FPGA* (5 to 40 k gates)

Six groups of microcontrollers

- 16-bit program counter
- 16-bit stack pointer
- Stack is at static RAM
- Initial default value defined in processor is 0x0000
- On-chip RAM (SDRAM)

AVR Microcontroller Architecture



AVR Architecture

- Thirty two general purpose registers (GPRs) of 8-bits associated with the 8-bit ALU.
- Six R26-R31 out of thirty 32 GPRs can be used as three 16-bit address registers.
- timer

AVR Internal Devices

- Serial SPI for synchronous serial communication, USART for serial synchronous-asynchronous receiver and transmitter and two wire serial interface (TWI)
- Two external interrupt pins, INT0 and INT1.
- ADC and analog voltage comparator
- Three timers-counters and watchdog timer

Ports and Interrupts

- Four Ports have data direction registers. This enables programming port pins as input or output.
- Nineteen interrupt levels, reset, INT0, INT1, timer interrupts for comparator, overflow and capture, interrupts for SPI and serial transfer complete, USART, ADC,

EEPROM, On-Chip Debugging and DAC

- EEPROM ready, analog-comparison, TWI and store program memory ready.
- On-chip debugging support with JTAG or Debug Wire (1-wire) interface (when flash is less than 16 kB).
- Classic version has no pulse width modulator and therefore support to DAC

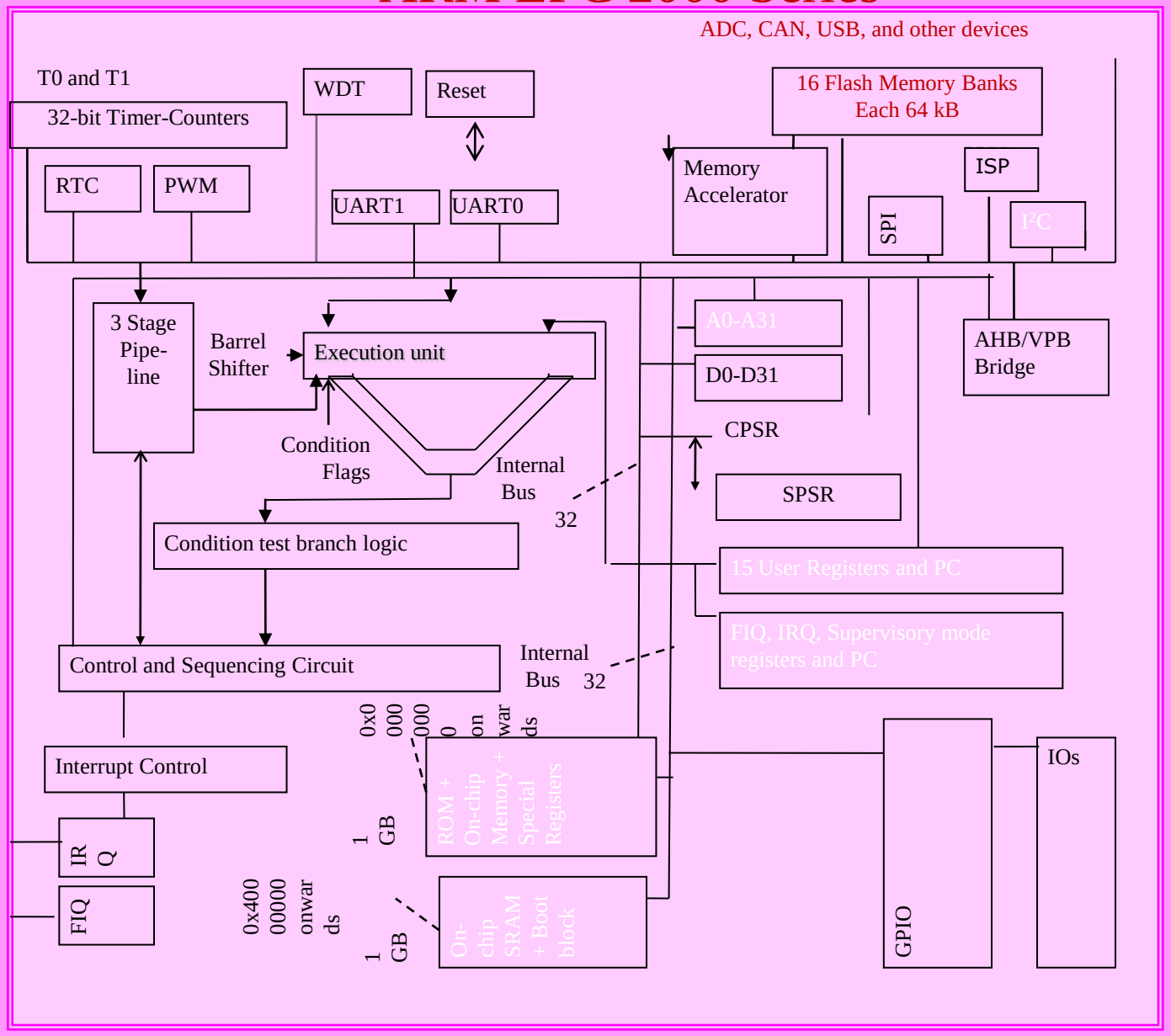
2. AVR® 32 microcontroller architecture

AVR® 32

- 32-bit arithmetic logic unit (ALU)
- 32-bit registers
- DSP instructions,
- SIMD instructions for supporting video processing.

3. ARM LPC 2000 Series microcontroller architecture

ARM LPC 2000 Series



ARM®

- stands for Advance RISC Machines (microprocessors)
- High performance at very low power consumption
- Family of RISC superscalar processor architecture for VLSI implementation
- Retains the best of CISC features also

ARM®

- The ARM“ VLSIs used widely as core or chip
- ARM MCUs (microcontrollers) manufactured by Philips (now Nexperia), ST Microelectronics and Samsung

ARM MCUs Hardware Units

- 1.8V internal, 1.8 V/2.5 V/3.3 V memory, 3.3 V operations
- Princeton and Harvard memory architecture,
- Running of the advanced RTOS such as Linux, WIN-CE, and QNX
- Combined SDRAM and cache for higher optimum performance

ARM MCUs Hardware Units

- Operations using 32-bitt ARM instruction set and 16-bit Thumb mode instruction set. This enables smaller storage for applications needing many 8-bit and 16-bit operations
- AMBA (advanced microcontroller bus architecture) MCU,

ARM MCUs Hardware Units

- IO port pins with four programmability: IO direction set for input or output, IO clear, IO set, IO (input-output) pin
- SPI, UART, I^2C (1-ch mtulti-master I^2C-BU S/1-ch I2S-BUS controller), I^2 BUS interface, SD 1.0 Host, external I/O microprocessor,
- Touch screen interface

ARM MCUs Hardware Units

- Timers with overflow, capture and compare control, watchdog timer , PWM, watch dog timer, PLL (phase locked loop circuit for generating constant frequency clock pulses),
- Highest performance embedded flash memory in 128-bit wide zero wait-state flash
- ADC and DAC

ARM MCUs Hardware Units

- Real time clock (RTC) with calendar function
- CAN controller in special versions

ARM MCUs Other Versions

- USB Host and USB/Client
- Ethernet
- 3 x SSC (Synchronous Serial Controller)
- 6 x timers
- Compact Flash

ARM MCUs Other Versions

- Smartmedia MMC Card
- SD Card
- Micro SD Card
- Burst Flash Controller

Summary

We learnt

- ATMEL AVR architectures
- AVR® RISC Harvard memory architecture microcontroller
- Four ports with data direction register with each, ADC, USART, SPI, TWI, three timer-counters

We learnt

- Two external interrupt pins, flash memory, EEPROM and SDRAM.
- Six groups of AVR® versions
- Possess for ADC, I^2C, CAN, USB, wireless ZigBee and other devices

We Learnt

- ARM LPC 2000 Series MCU
- Consists of high performance at very low power consumption
- AMBA (advanced microcontroller bus architecture) as high speed IOs
- SPI, UART, I^2C (1-ch mtulti-master I^2C-BUS/1-ch I^2C-BUS controller)

We Learnt

- I^2C BUS interface
- SD 1.0 Host, external I/O microprocessor,
- Touch screen interface
- ARM Flash memory and in-system programming. JTAG debugging interface enables debugging the system in development phase

End of Lesson 5 of Chapter 3 on ATMEL, AVR ® AND ARM Microcontrollers