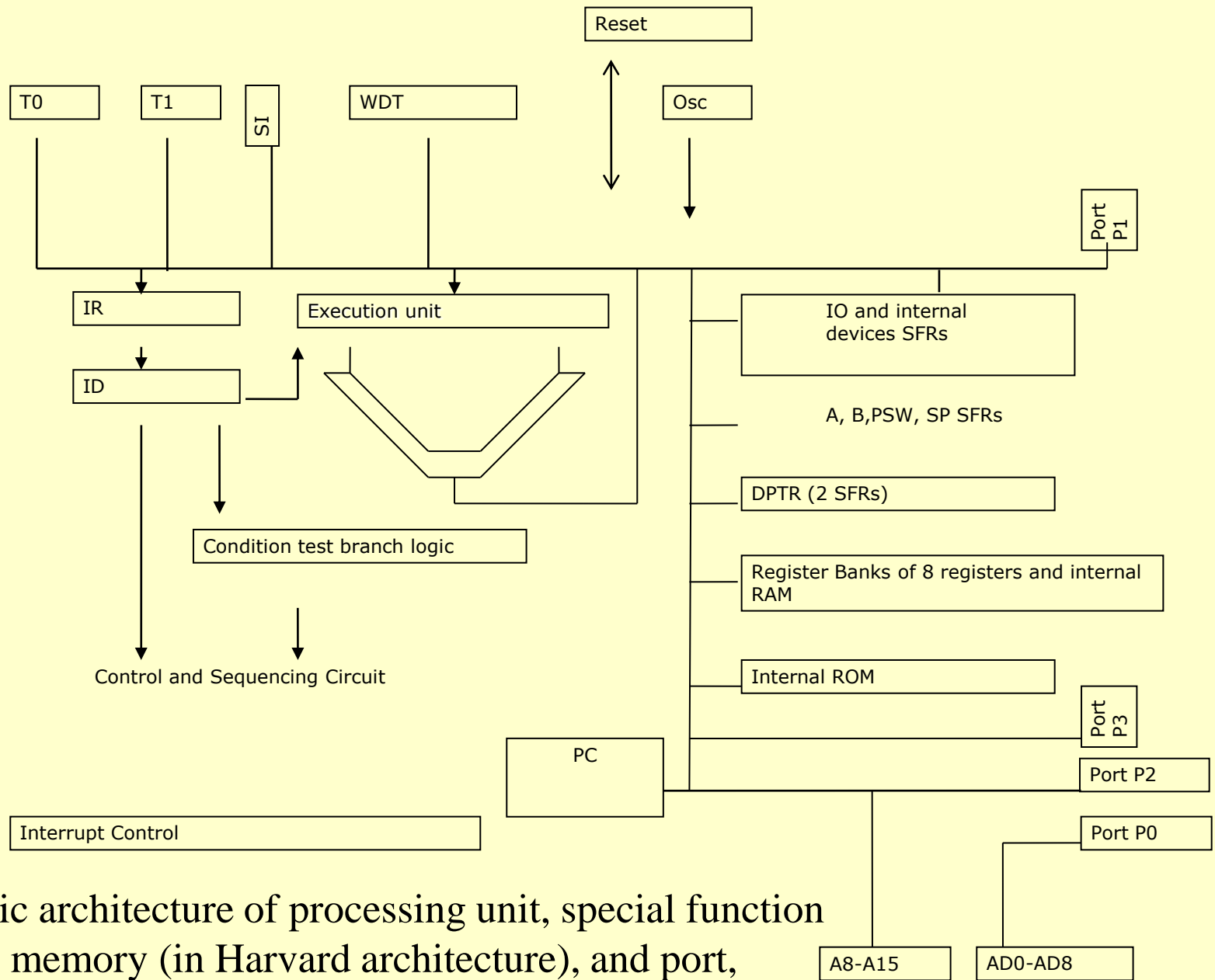


8051, AVR, ARM MICROCONTROLLERS AND REAL WORLD INTERFACING AND

IOs USING BUSES –

Lesson-1: 8051 Architecture, Instruction Set and Interrupts

1. 8051 microcontroller architecture



8051 basic architecture of processing unit, special function registers, memory (in Harvard architecture), and port, counters/timer, watch dog timer, serial IO and interrupt handler devices

8051 microcontroller features

- 12 MHz clock. Processor instruction cycle time 1 μ s. [in Classic version]
- 8-bit ALU
- Harvard memory architecture – the external program memory and data memory have separate address spaces from 0x0000 and separate control signal(s).
- 8-bit internal data bus width and 16-bit internal address bus – Harvard memory architecture
- CISC (Complex Instruction Set Computer)

8051 microcontroller features (contd.)

- Special function registers (SFRs) –PSW (processor status word), A (accumulator), B register, SP (stack pointer) and registers for serial IOs, timers, ports and interrupt handler.

8051 microcontroller features (contd.)

- Special bit manipulation instructions.
- 16-bit Program counter with initial default reset value defined by processor is 0x0000.
- 8-bit stack pointer with initial default value defined by processor is 0x07

8051 microcontroller features (contd.)

Classic 8051 simple architecture

- no floating-point processor,
- no cache,
- no memory management-unit,
- no atomic operations unit,
- no pipeline and
- no instruction level parallelism.

8051 microcontroller features (contd.)

- on-chip RAM of 128 bytes. [8052-version RAM 256 bytes.]
- 32 bytes of RAM also used as four banks (sets) of registers. Each register-set (bank) thus eight registers.
- External data/stack memory can be added upto 64 kB in most version. In certain 8051 enhancements, this limit enhanced to 16 MB

8051 microcontroller features (contd.)

- 8351 version on-chip ROM, 8751 version EPROM, 8951 version has on-chip EEPROM or flash memory of 4 kB.
- Several versions provide for higher capacity ROM. Additional program memory can be added externally upto 64 kB. In extended 8051 and unified address space versions (8051 EX and MX versions), this limit has been extended to 16 MB.

8051 microcontroller features (contd.)

- Two external interrupt pins, INT0 and INT1.
- Four ports of 8-bits each in single chip mode.
- Two timers
- Serial interface (SI)—programmable for three full duplex UART modes for serial IO. [IO with each bit of a word successive transmission on the data line for a time interval.] The same be programmable for half duplex synchronous IO

8051 microcontroller features (contd.)

- In certain versions – DMA controller
- In certain versions– pulse width modulator and thus support to DAC, d.c. and servo motor controls.
- In Certain versions – modem, watchdog timer, ADC. Siemens SAB 80535-N supports ADC with programmable reference voltage. Advanced versions support these features and a version is selected as per the system requirement

2. 8051 microcontroller instruction set

Data Transfer Instructions

- Move byte between accumulator (an SFR) and register at a register bank
- Move byte from an SFR/Internal RAM to another *direct*
- Move *indirect*
- Move *immediate*, MOV *immediate* DPTR
- MOVC and MOVX *indirect*
- Exchange or Push or Pop *direct*

Bit and Byte Manipulations and Logic instructions

Bit Manipulation

- Set, Complement, AND or OR or MOV the bit

Logic Instructions

- AND, XOR, OR Operation Instructions

Byte Manipulation

- Clear, Complement, or swap and Rotate Instructions

Arithmetic Instructions

- 8-bit Add, Subtract, Multiply and divide Instructions
- Increment-Decrement Instructions

Program Flow Control Instructions

- Branch instructions
- Conditional jumps
- Decrement and Jump conditional
- Compare and then conditional jump
- Subroutine Call Instructions
- NOP
- Delay

Interrupt Flow Control Instructions

- Interrupt flow control- mask bits, priority bits
- RETI

3. 8051 Hardware Interrupts

Interrupt Sources

- External INT0 interrupt
- T0 overflow interrupt
- External INT1 interrupt
- T1 overflow interrupt
- SI serial UART or Synchronous mode interrupt
- SI synchronous serial mode interrupt (separate in few families of 8051)
- Timer 2 interrupt in 8052

SFR IE for interrupts enabling bits

SFR to mask (disable) or unmask (enable) the interrupts in 8051

- Programming of SFR IE (Interrupt Enable) register at address 0xA8 for the byte or
- Programming of IE using Bit addresses 0xA8 to 0xAF for the individual bits

SFR IP for interrupt priority bits

- Individual interrupt priorities set high or low bits
- Set priorities in IP override default priorities for executing the ISRs
- Byte address 0xB8 for the byte and at bit addresses 0x88 to 0x8C or 0x8D or 0x8E for the individual bits in the register, an instruction can define that a given interrupt is of higher (=1) or lower priority (=0) among the various interrupts

8051 system Interrupt Features

- 8051 permits when executing low- priority ISR the in-between program flow on interrupt to higher priority ISR
- Permits masking all by a primary level bit or individual sources by secondary level bits by setting bits in SFR IE
- Assigns default priorities
- Permits overriding of default priorities by setting bits in SFR IP

Vector Addresses

- An address from where either an ISR of maximum 8-bytes executes or a Jump to a programmed ISR starting address takes place
- When EA bit (primary level interrupt bit) is set as well as specific interrupt bit (secondary level interrupt bit) is set

External hardware Interrupts

INT0 and INT1

programmable for

- Two external interrupt pins, INT0 and INT1 at P3.2 and P3.3 used for interrupt
- P3.2 and P3.3 as pins for INT0 and INT1 external interrupt pins when bit 7 IE (interrupt enable SFR) EA (enable all) bit is 1, and bits 0 and 2 are 1 and 1, respectively
- Programmed by TCON lower 4 bits and the IE register bits IE.2 and IE.0

INT1 and INT0 status bits

- Status bit TCON.3 for status of interrupt at INT1
- TCON.3 auto resets to 0 when ISR for servicing INT1 interrupt starts.
- Status bit TCON.1 for status of interrupt at INT0 and
- TCON.1 auto resets to 0 when ISR for servicing INT0 starts.

INT1 and INT0 Edge or level type control bits

- TCON.2 for type of interrupt at INT1 and is 1 if it is edge-triggered type else 0.
- TCON.0 for type of interrupt at INT0 and is 1 if it is edge-triggered type else 0.

INT0	0x0003
T0	0x000B
INT1	0x0013
T1	0x001B
Serial	0x0023
T2	0x002B
Syn Serial	0x0053 in few versions

↑ High
 Default Priorities
 by hardware
 (Software
 assigned high
 priority setting in
IP overrides the
 default)
 ↓ Low

Vector Addresses and Default priorities

Summary

We learnt

- 8051 architecture
- Instruction set of 8051

We learnt

- Interrupt sources
- Interrupt system features
- Vector addresses
- Default priorities
- SFR IE for enabling all and enabling individual sources
- SFR IP for setting priority low or high for individual sources of interrupts

End of Lesson 1 of Chapter 3
on
8051 Architecture, Instruction Set and
Interrupts