

Chapter 14 Embedded Software development Process and Tools

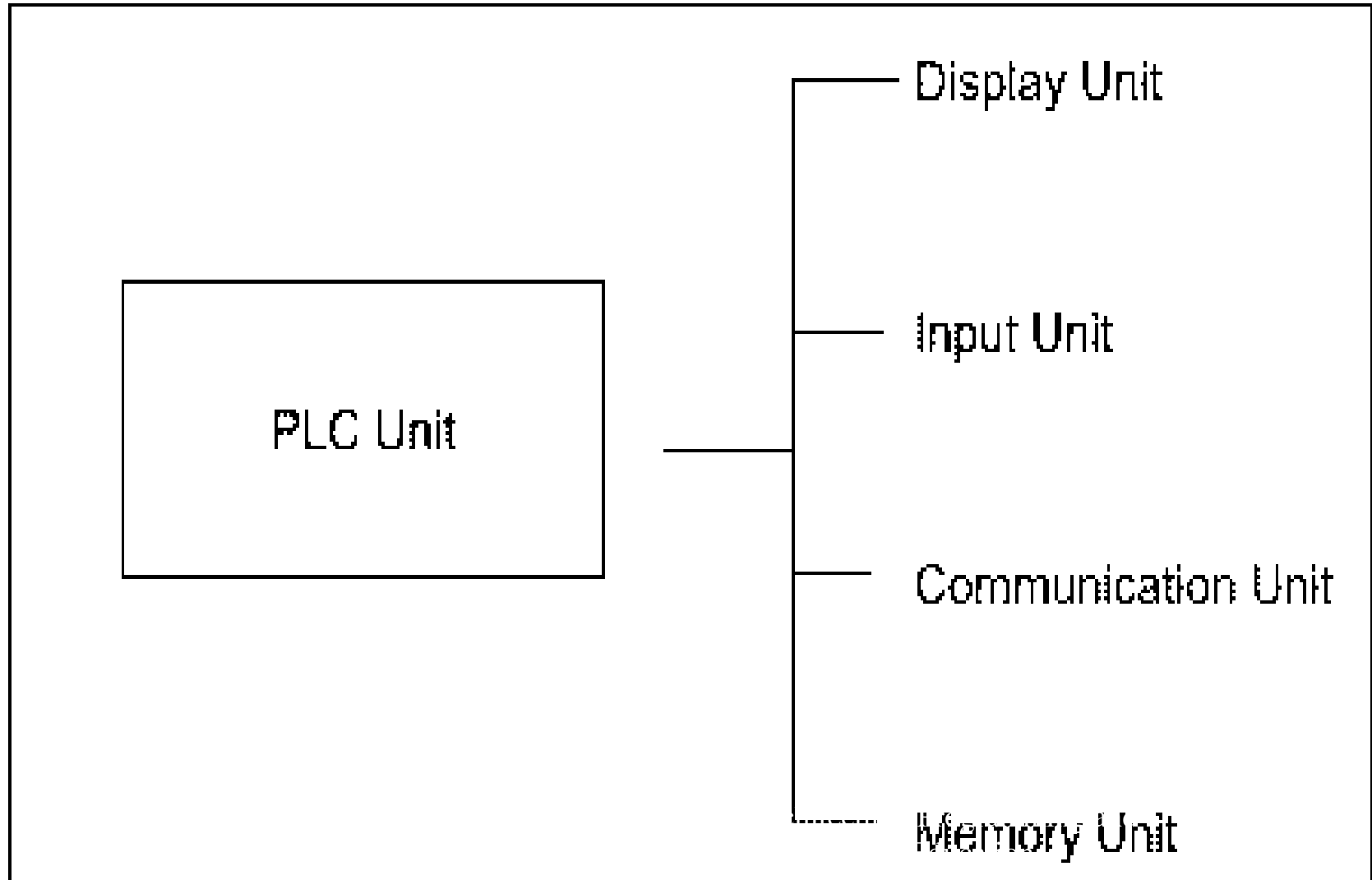
Lesson-6: Issues in Hardware and Software Design and Co-Design

1. Choice of Right Platform

- Processor Less System

System Platform

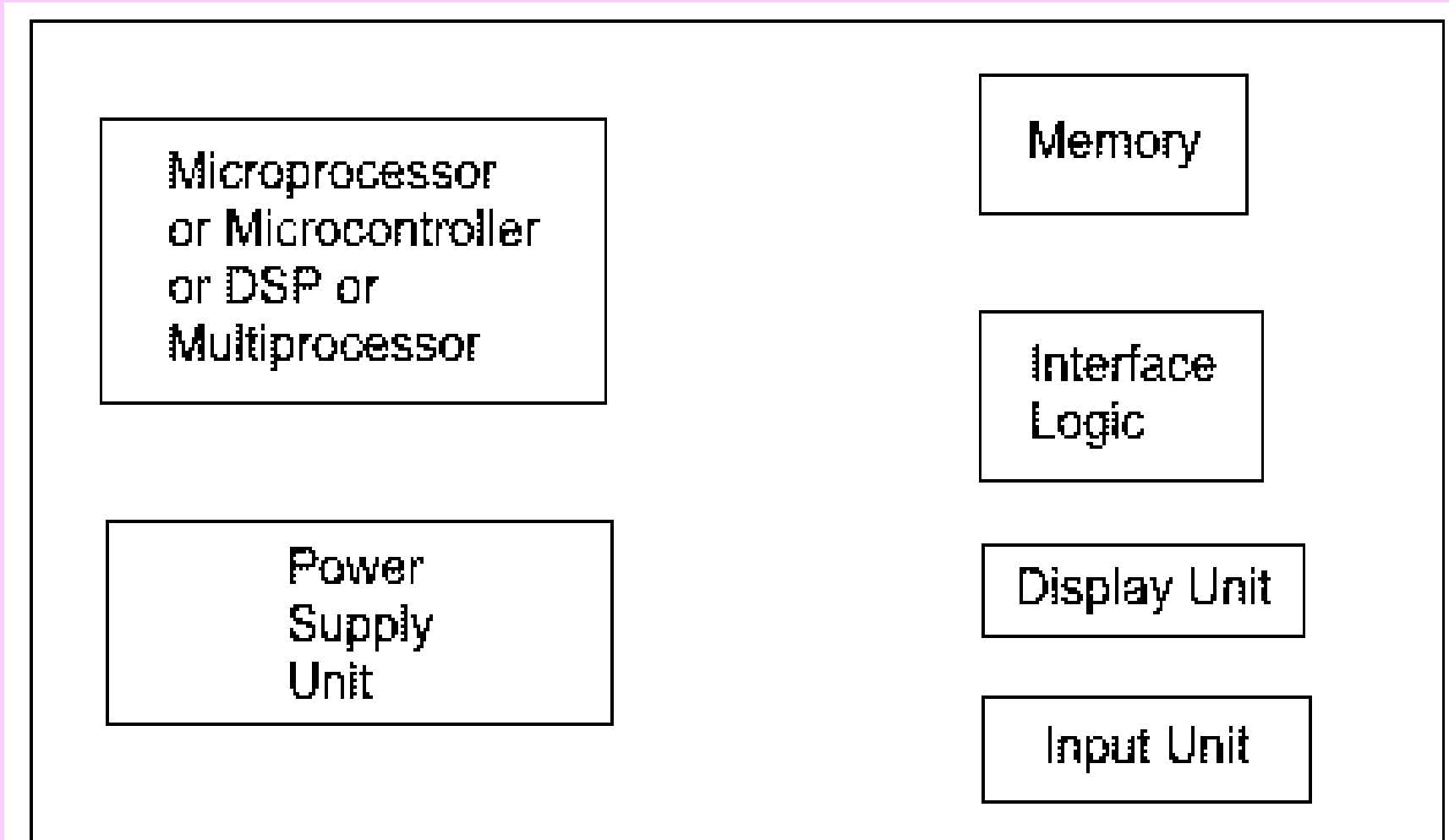
PLC (Programmable logic unit) instead
of Processor



System Platform

- Processor Based System

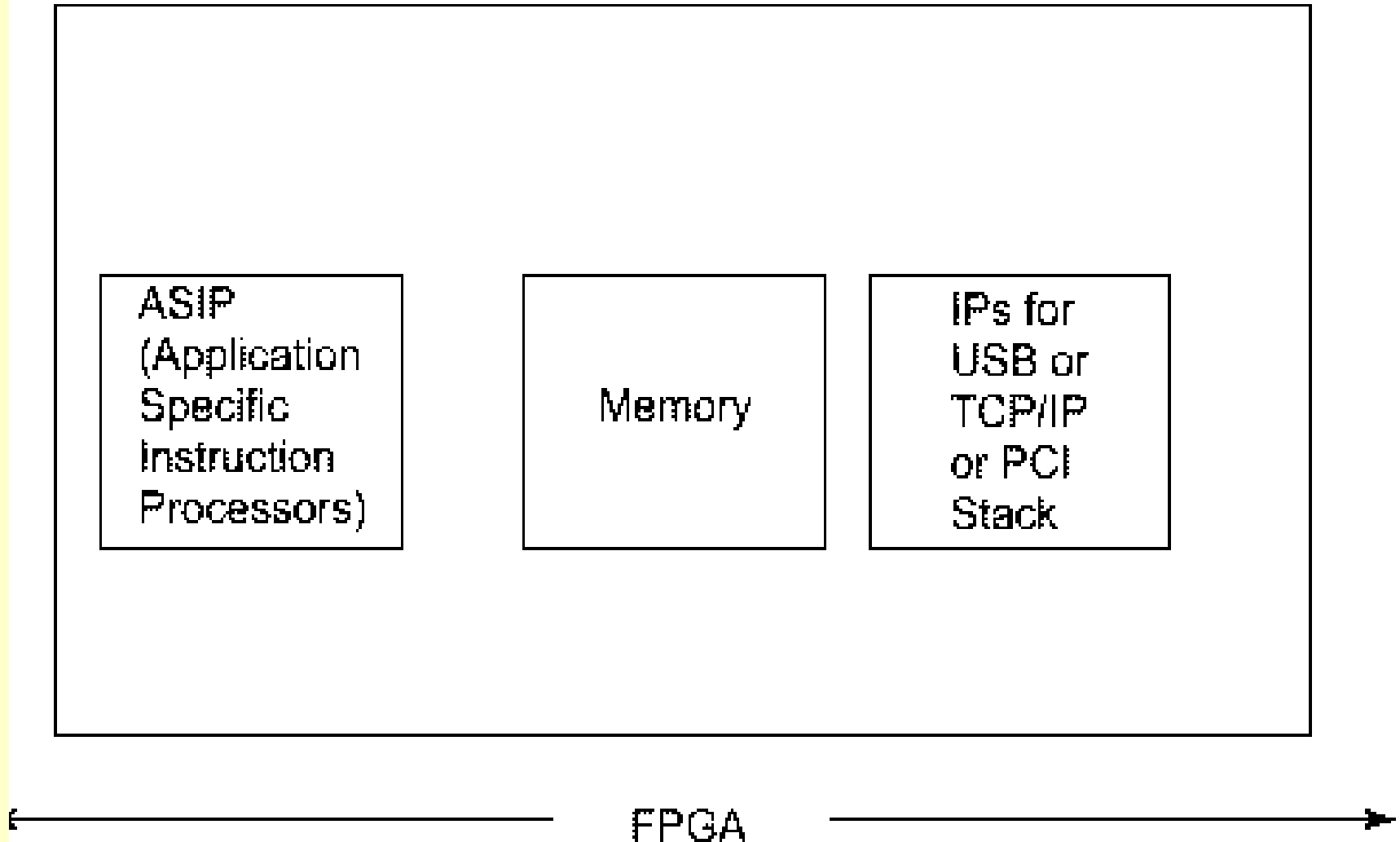
Microprocessor or Microcontroller or DSP based system



System Platform

- IP or FPGA Based System

IP and FPGA based system



2. Software-Hardware Tradeoff

- 1) Certain subsystems in hardware (microcontroller), real-time clock, system clock, pulse width modulation, timer and serial communication can also be implementable by software.

Software-Hardware Tradeoff ...

- 2) Hardware implementations though increase the operation speed but may increase power requirements.

Software-Hardware Tradeoff ...

- 3) A serial communication, real-time clock and timers featuring microcontroller may cost more than the microprocessor with external memory and a software implementation
- 4) Simple coding for device drivers

Software implementation advantages

- (i) Easier to change when new hardware versions become available
- (ii) Programmability for complex operations
- (iii) Faster development time
- (iv) Modularity and portability

Software implementation advantages

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- (v) Use of standard software engineering, modeling and RTOS tools.
- (vi) Faster speed of operation of complex functions with high-speed microprocessors.
- (vii) Less cost for simple systems

3. Performance Accelerators

- 1) Conversion of CDFGs into DFGs for example by using loop flattening (loops are converted to straight program flows) and using look-up tables instead of control condition tests to decide a program flow path

Performance Accelerators ...

- 2) Reusing the used arrays in memory, appropriate variable selection, appropriate memory allocation and de-allocation strategy

Performance Accelerators ...

- 3) Using stacks as data structure when feasible in-place of queue and using queue in place of list, whenever feasible.
- 4) Computing slowest cycle first and examining the possibilities of its speed-up.

Performance Accelerators ...

- 5) Code such that more words are fetched from ROM as a byte than the multi-byte words

4. Hardware implementation advantages

- (i) Reduced memory for the program
- (ii) Reduced number of chips but at an increased cost
- (iv) Internally embedded codes, more secure than at the external ROM.

Performance Accelerators ...

- An accelerator may include bus interface unit, DMA, read and write units, registers and accelerator cores.
- An accelerator uses a programming model to accelerate, unlike the coprocessor, which has instruction sets for specific tasks.

Performance Accelerators ...

- A processor registers interact and connect to an accelerator through buses so that processor controls the accelerator for obtaining a higher performance.

Performance Accelerators ...

- Example - JA108 from Nazonin Communications, a Java accelerator, which accelerates the JAVA code run by 15 to 60 times.
- Another example is a video accelerator, which accelerates video processing tasks.

Performance Accelerators ...

Hardware accelerator accelerates code execution. It may be an ASIC, IP core or FPGA.

5. Porting IO Instructions issues of in an Embedded Platform

- Data type may be different on the different platforms, as follows:
- (i) unsigned char* (PowerPC, M68HC11/12, M68K, S390),
- (ii) unsigned int (ARM)
- (iii) unsigned long (Itanium, Alfa, SPARC)
- (iv) unsigned short (80x86)

Interrupt Vectors OS support

- Interrupt vectors are to be defined differently
- OS supports these differently on different platforms

6. Interface Addressing Issues

- For example, a network interface card supports 32-bit unsigned integers and with a big endian.

7. Data Alignment

- (i) Two or three bytes stored at an address from which processor accesses 4-bytes in an access.

Data Alignment...

- (ii) Same data structure at 'C' source file may show differently on different platforms. ['C' takes 16-bit integer on a 16-bit processor and 32-bit integer on a 32-bit processor].
- Compiler must force the alignment of data by the OS-hardware interface function

Summary

- (i) Choice of Platforms
- (ii) Software-Hardware Tradeoff
- (iii) Software methods and hardware Performance accelerators to improve the performance
- (iv) Porting Issues

We learnt

- Data Type and Data Alignment
Issues

End of Lesson-6 of Chapter 14 on “Issues in Hardware and Software Design and Co-Design”