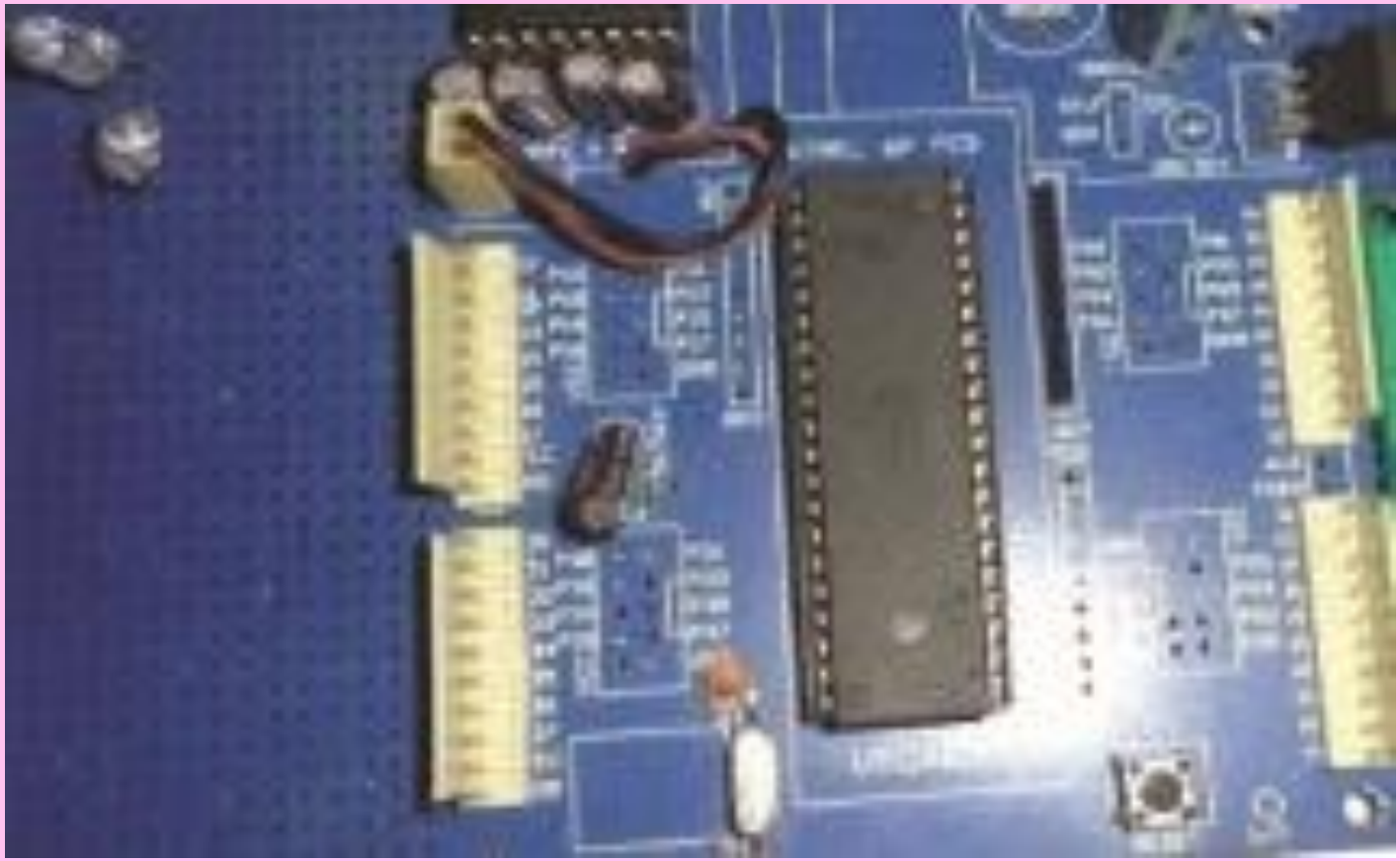
Lesson 01: SYSTEM-ON-CHIP (SoC) AND USE OF VLSI CIRCUIT DESIGN TECHNOLOGY

VLSI chip

- Integration of high-level components
- Possess gate-level sophistication in circuits above that of the counter, register, multiplier, floating point operation unit and ALU.

Circuit on Board



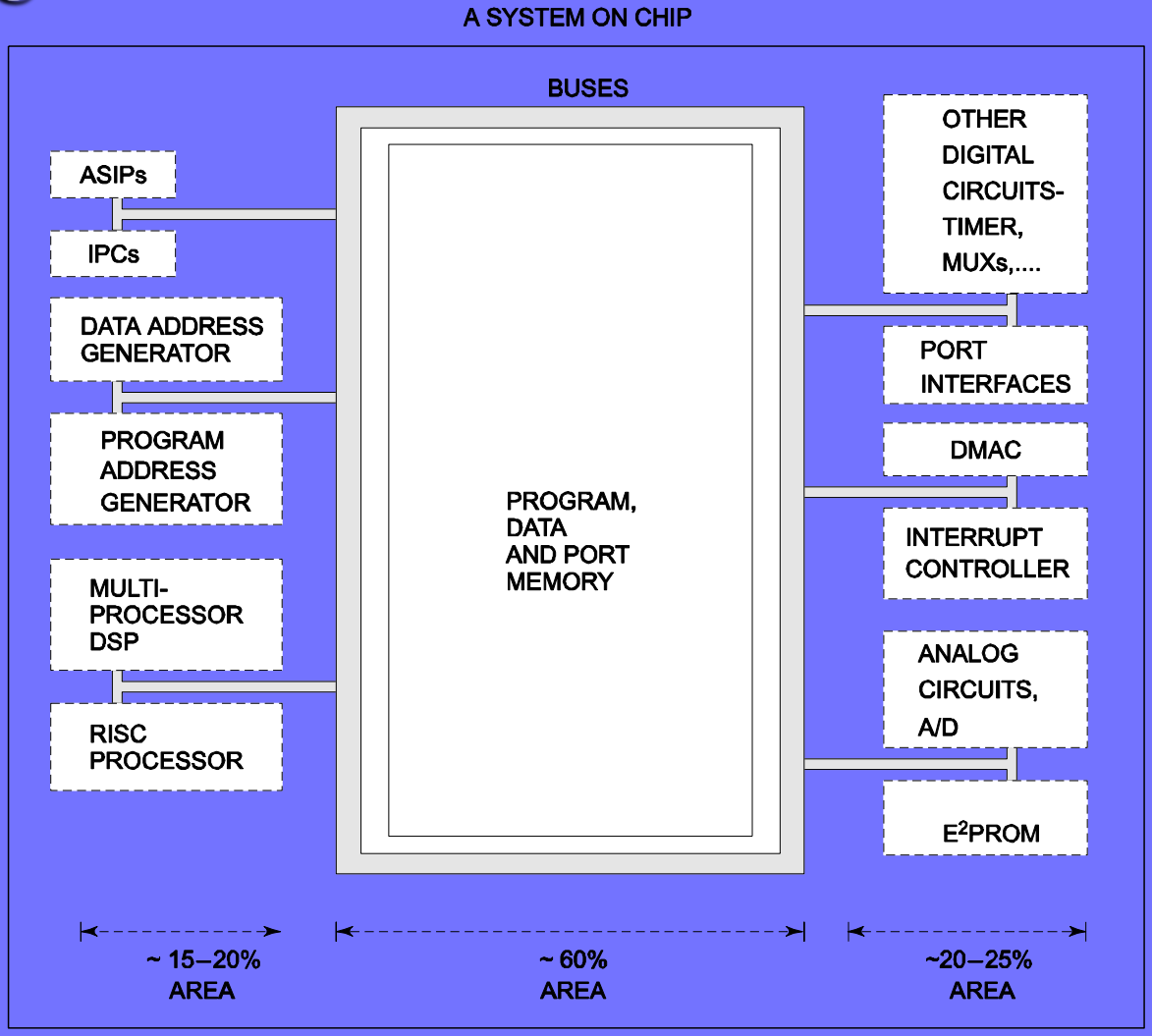
System on chip (SoC)

- A design innovation
- A system on a VLSI chip that has all needed analog as well as digital circuits, processors and software

SoC

Multiple Processors, ASIPs, IPs, ASICs, Cache, RAM, IPs, Logic and Analog Circuits on a single chip

New Innovation Example – Mobile Phone on a SoC



SYSTEM-ON-CHIP

Embeds:

- Multiple processors,
- Memories,
- Multiple standard source solutions (IP Cores),
- Logic and analog units

Embedding Multi-processor or Dual Core using General Purpose Processors (GPPs)

- Speech signal-compression and coding.
- Signal decoding and decompression.

Embedding an Accelerator

- Accelerate the execution of codes
- A floating point coprocessor accelerates the mathematical operations and
- Java accelerator accelerates the Java code execution.

Embedding Single purpose processors

- For Dialing, Modulating, Transmitting. Demodulating and Receiving
- Keypad interface and display interface handling.
- Touch screen
- Message display and creation, SMS (Short Message Service) and MMS
- Protocol- stack generation.
- Pixel coprocessor and CODEC in a digital camera

Embedding Microprocessors

- General Purpose Processor (GPP) microprocessors

Embedding an ASIPs

- Processors with instruction set designed for specific set of applications on a VLSI chip, for example, microcontroller, DSP, IO, media, network or other domain specific processor

Embedding Microcontroller cores

- 80251
- PIC 16F84 or 16C76, 16F876 and PIC18Microcontroller
- Enhancements of ARM9/ARM7 ARM Cortex M series

Embedding DSP Cores

- TMS320Cxx, OMAP1Tiger SHARC 5600xx PNX 1300, 15002
- Image, video, signals processing
- Filtering, noise cancellation, echo elimination, compression and encryption

SoC

- Embedded processor GPP or ASIP core,
- Single purpose processing cores or multiple processor cores,
- A network bus protocol core,
- An encryption and decryption functions cores,
- Cores for FFT and Discrete cosine transforms for signal processing applications,
- Memories

SoC (Contd.)

- Multiple standard source solutions, called IP (Intellectual Property) cores,
- Programmable logic device and FPGA (Field Programmable Gate Array) cores.
- Other logic and analog units.

IPs in SoC

- IP –a standard source solution for synthesizing a higher-level component by configuring a core of VLSI circuit or FPGA core available as an Intellectual Property, called (IP).
- High Level Components with gate level sophistication circuit much above level of counters and registers.

IPs

- Designer or designing company holds the copyright for the synthesized design of a higher-level component for gate-level implementation of an IP.
- One might have to pay royalty for every chip shipped. An embedded system may incorporate several IPs.

IP

An IP may provide a

- design for adaptive filtering of a signal.
- full design for implementing Hypertext Transfer Protocol (HTTP) or File Transfer Protocol (FTP) to transmit a web page or file on Internet.
- USB port controller, Bluetooth, GPS interface, Wireless 802.11or 802.16 interfaces

FPGA Core

- An FPGA consists of a large number of programmable gates on a VLSI chip. There is a set of gates in each FPGA cell, called 'macro cell'.
- Embedded system designed with a view of offering enhancing functionalities in future, then FPGA core can be used in the circuits.

FPGA Core

- Each cell has several inputs and outputs. All cells interconnect like an array (matrix).
- Each interconnection is programmable through the associated memory RAM in a FPGA programming tool.
- A concept is using FPGA (Field Programmable Gate Arrays) core along with single or multiple processors.

FPGA

- An SIMD instruction, Fourier transform and its inverse, DFT or Laplace transform and its inverse, compression or decompression, encrypting or deciphering, a specific pattern-recognition (for recognizing a signature or finger print or DNA sequence).
- Configure an algorithm into the logic gates of the FPGA.

Summary

We learnt

- Subunits in SoC- embedding ASIPs, IPs, ASICs, Cache, RAM, IPs, Logic and Analog Circuits on a single chip

End of Lesson 01