Chapter 11: Input/Output Organisation

Lesson 03:

Synchronous data transfer

Objective

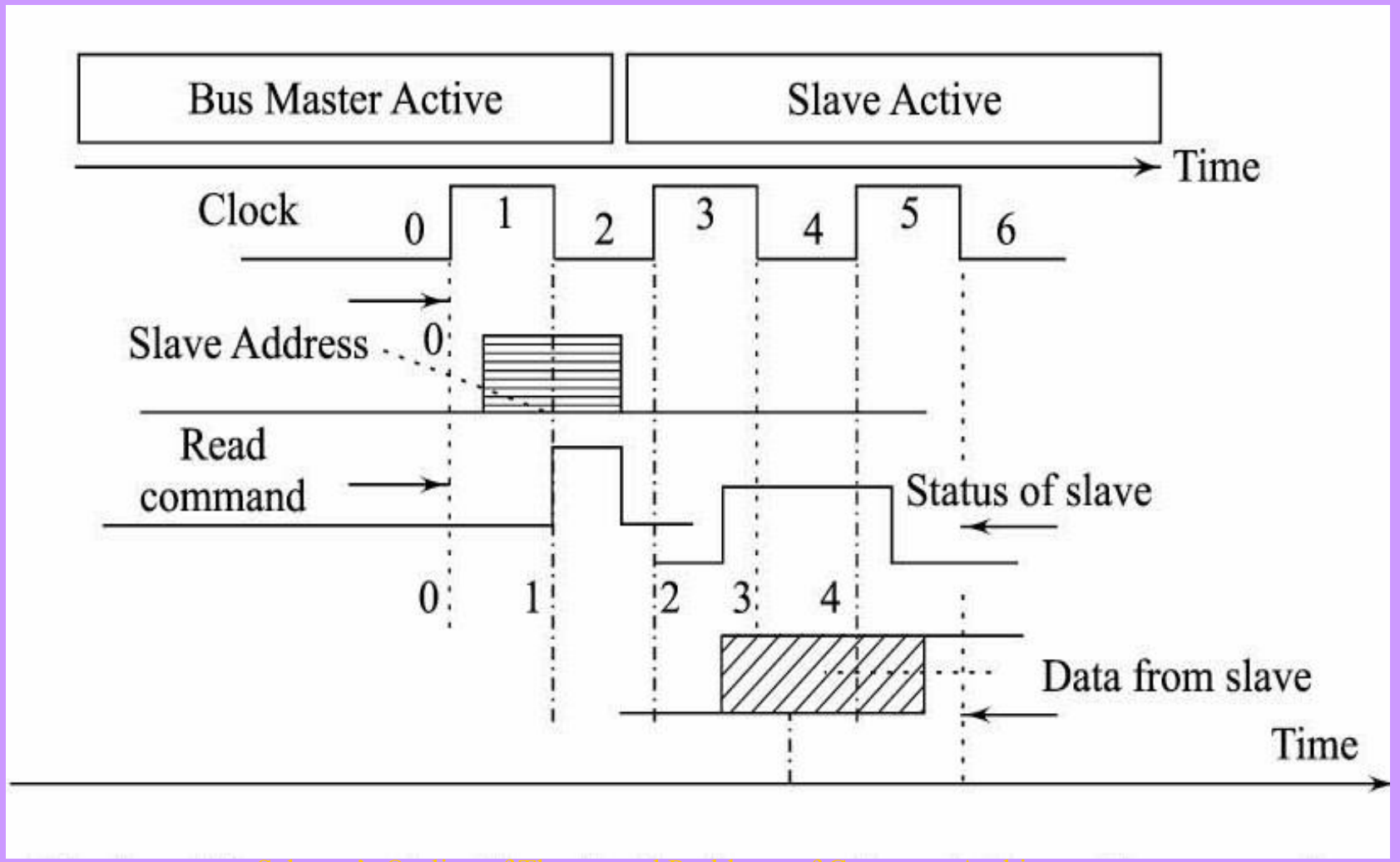
- Understand the data transfer on synchronous bus
- Learn the synchronous parallel and serial transfer
- Learn the timing of the various signals guided by the master clock in synchronous bus
- Understand that slaves must synchronize their internal clock and actions with the master in the synchronous transfer

Synchronous data transfer

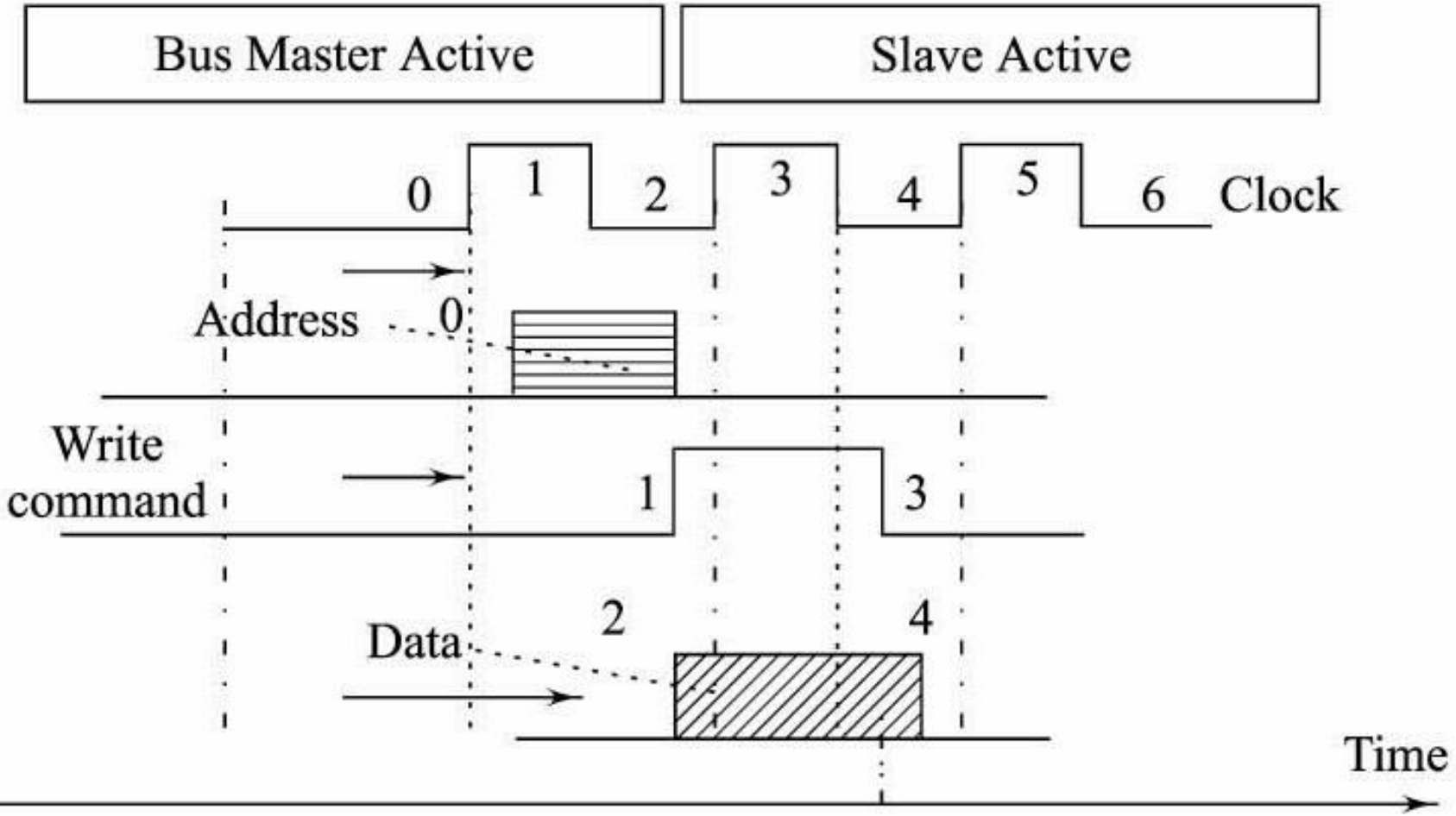
Data transfer

- Synchronous data transfer using synchronous bus
- Parallel and serial transfer

Synchronous data transfer during read



Write operation using synchronous bus



Synchronous data transfer Input operations

The timing of the various signals guided by the master clock in synchronous bus

1. *Sequence 0*: Guided by the master clock, the master (initiator) sets the address (in time t_{set}) bits and sends an address or command, which reaches the slave (target) in time t_{elec} (due to wire length and transmission line or other effects) after setting the bits on the address or command bus (may or may not be same as data bus

The timing of the various signals guided by the master clock in synchronous bus

2. *Sequence 1*: Guided by the master clock, the master sets the command (read control signal), and the slave then sets the status (address or command) in time t_{set} and sends to the master in time t'_{elec} after setting

The timing of the various signals guided by the master clock in synchronous bus

3. *Sequence 2*: Guided by master clock, the master reads and receives the slave's status bits

The timing of the various signals guided by the master clock in synchronous bus

4. *Sequence 3*: The slave sets the data bits in time t''_{set} and in time t''_{elec} after setting sends the bits to the master

The timing of the various signals guided by the master clock in synchronous bus

5. *Sequence 4*: Guided by master clock, the master reads and receives these bits

Slaves synchronization

- Slaves must synchronize their internal clock so that sequence 1 action must complete before sequence 2
- The slave must synchronize its internal clock so that sequence 3 actions must complete before sequence 4

Waiting period between sequence 1 and 2

- There may be a waiting period between sequence 1 and 2 in case the slave is a slow device compared to the master clock period
- However, instead of taking place in next clock cycle, sequence 2 and 3 must take place after a fixed wait of the *m* clock cycles

Synchronous data transfer Output operations

The timing of the various signals guided by the master clock in synchronous bus

1. *Sequence 0*: Guided by the master clock, the master (initiator) sets the address (in time *t*set) bits and sends an address or command, which reaches the slave (target) in time *t*elec (due to wire length and transmission line or other effects) after setting the bits on the address or command bus (may or may not be same as data bus).

The timing of the various signals guided by the master clock in synchronous bus

2. *Sequence 1*: Guided by the master clock, the master sets the command write control signal and sends the write control bit

The timing of the various signals guided by the master clock in synchronous bus

3. *Sequence 2*: Guided by the master clock, the master sets the data in time t'_{set} and sends them to the slave in time t'_{elec} after setting the write control bit

The timing of the various signals guided by the master clock in synchronous bus

4. *Sequence 3*: Slave writes the data bits after a time t''_{set} into its latch, which is after receiving the bits from the master in time t''_{elec}

The timing of the various signals guided by the master clock in synchronous bus

5. *Sequence 4*: Guided by the master clock, the master deactivates the data bus signals

Slaves synchronization of their internal clock

- Slaves must synchronize their internal clock so that sequence 1 control signal action completes before sequence 2 starts
- Slaves must synchronize their internal clock so that sequence 3 actions complete before sequence 4 actions begin

Summary

We Learnt

- Synchronous parallel and serial transfer
- The timing of the various signals guided by the master clock in synchronous bus
- Slaves must synchronize their internal clock with the master inn synchronous transfer

End of Lesson 03 on

Synchronous data transfer