Chapter 08: The Memory System

Lesson 09:

DRAM access controller and Refresh Logic Control

Objective

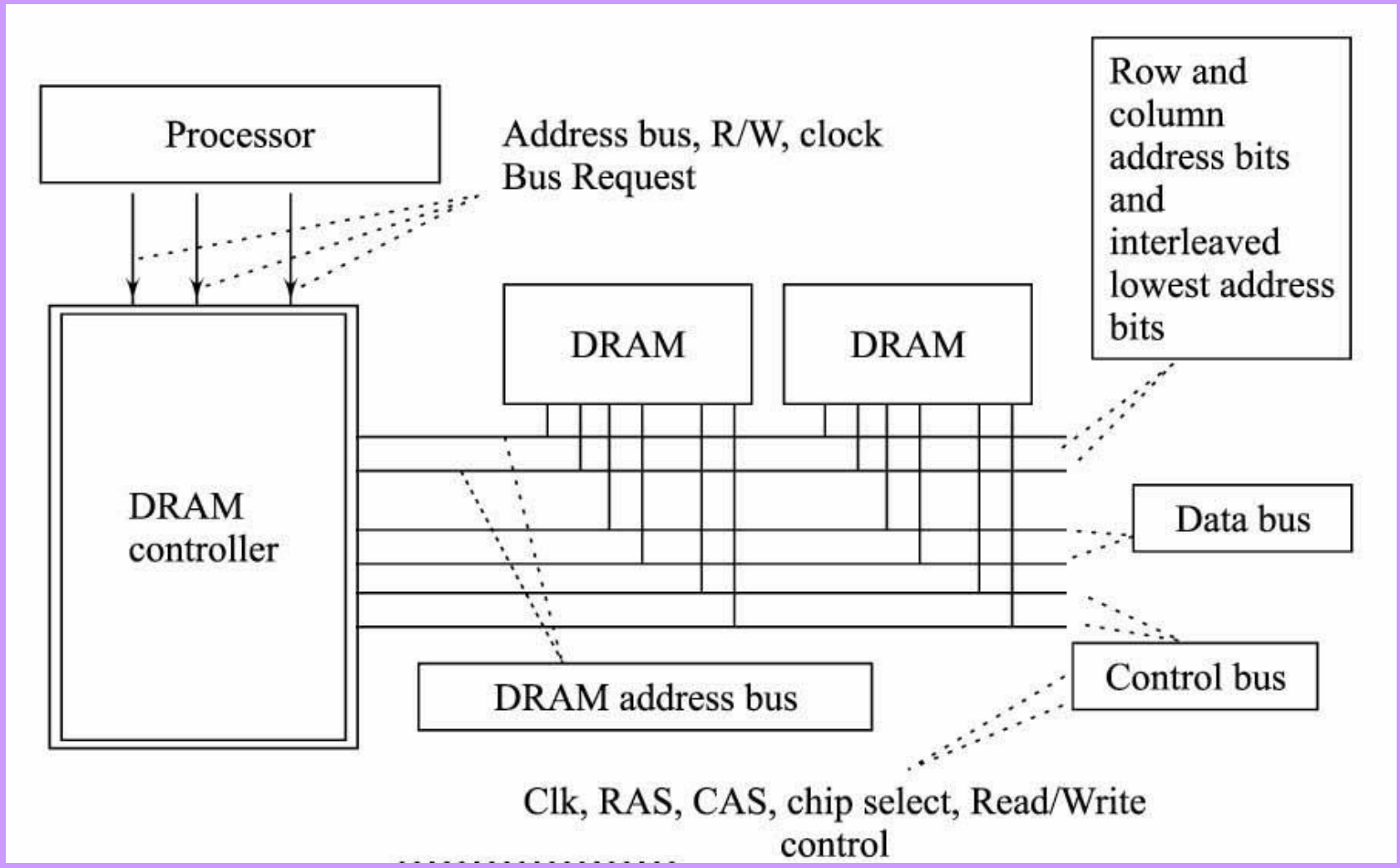
- Understand the functions of DRAM access controller
- Understand Refresh control logic

DRAM access controller

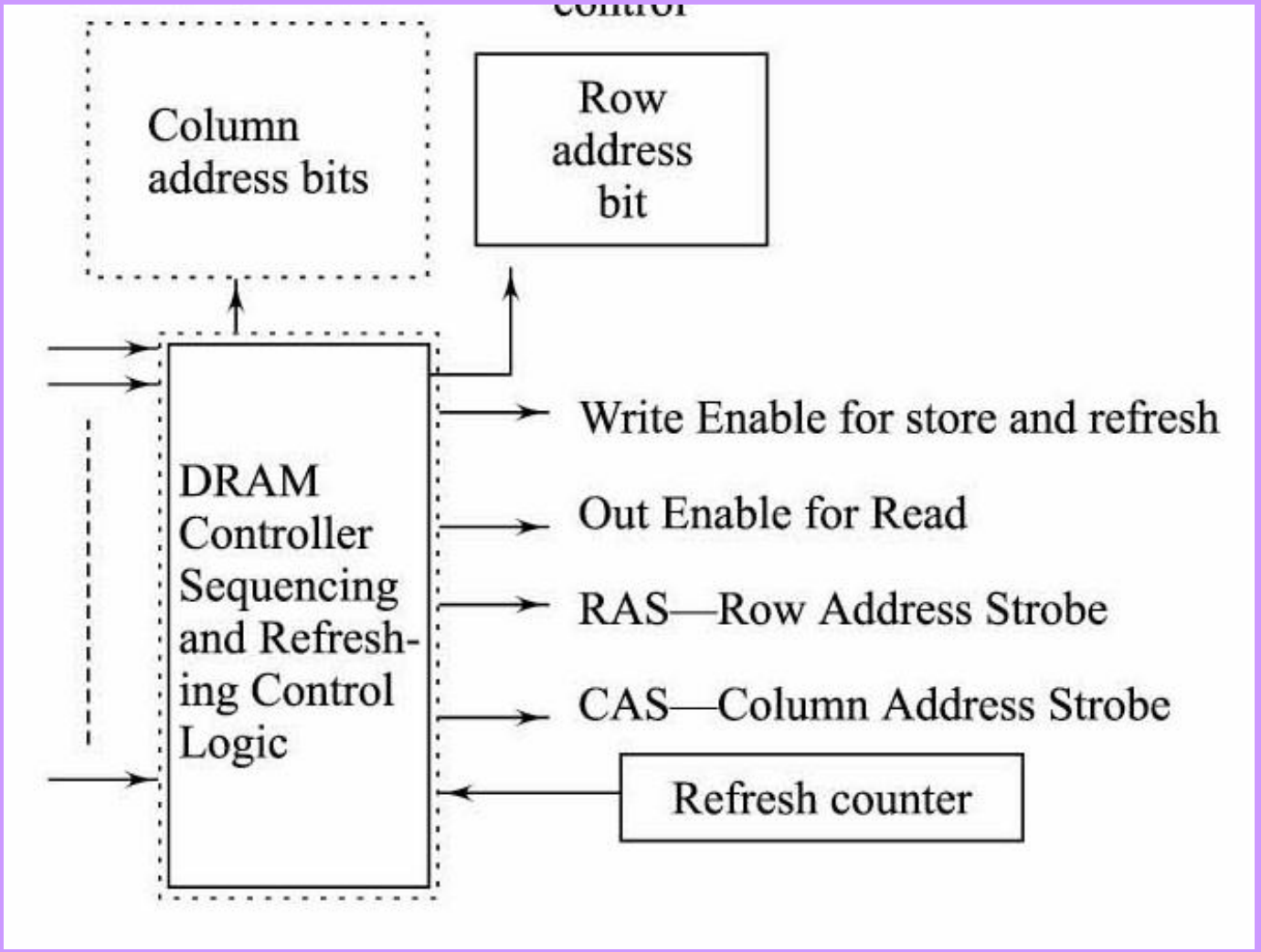
DRAM controller

- Issues RAS and CAS signals, chip select, and DRAM clock
- The number of pins connecting the DRAM is one of the considerations
- The address issued by the processor multiplexed at a DRAM controller to generate the row address bits and column address bits

DRAM Controller



DRAM control Sequencing and refresh logic



Example

- Assume a DRAM has 4096 rows in its array of bit cells and a refresh time of 2 ms
- Each row must be refreshed once every refresh time, so 4096 row-refresh operations must be done every 2 ms
- 1 row refreshes every 480 ns on average
- Assume that each row-refresh process at the DRAM takes 4.8 ns

Fraction of the DRAM'S time taken by row refreshes

- = 4.8 ns/480 ns = 1.0 percent
- Refresh overhead is negligible compared to the overhead in accessing the cells of DRAM

Summary

We learnt

- DRAM controller, sequencer and refresh logic functions

End of Lesson 09 on

DRAM access controller and Refresh Logic Control