

Chapter 06: Instruction Pipelining and Parallel Processing

Lesson 08: Instruction Set Design Influence on Pipelining

Objective

- Learn how an instruction set design influence the pipeline

Simple addressing mode Influence

Simple addressing modes

- Register addressing— No address calculation needed
- Register indirect addressing mode (ri)— No address calculation by processor needed
- Index addressing mode $x(ri)$ — Just one cycle needed for address computation

Advantages during pipelining of instructions with simple addressing modes

- No effect on other instructions to cause instruction hazards
- Just one cycle memory access needed for address

Load and Store Architecture Influence

Advantage

- Memory access needs only by the load and store instructions

Complex addressing mode Influence

Complex Addressing Modes

- Index with increment or decrement addressing modes $x[ri]$ or $(ri) +$
- Need of address calculation
- Need to write back the calculated address for modifying the ri
- Memory indirect with offset

Disadvantages during pipelining

- Consider instruction — I_n as LD $rj, [(x(ri))]$
- Needs seven pipeline stages
 - (1) Fetch
 - (2) Decode
 - (3) Read operands x and ri ,
 - (4) Calculate read memory address

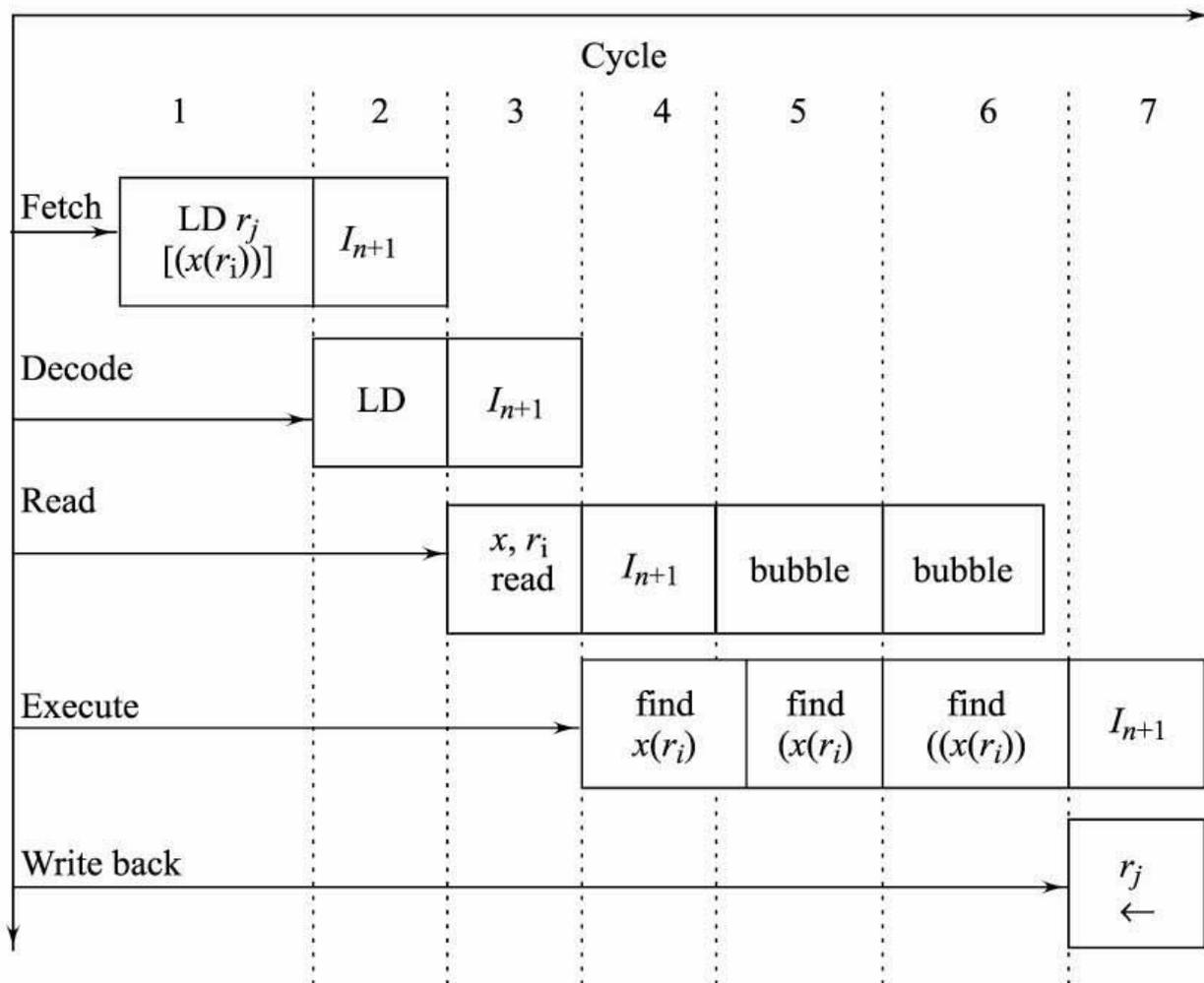
Disadvantages during pipelining

- (5) Access memory address operands from $x + r_i$
- (6) Make another memory access fetch the source operand
- (7) Write back the source operand to destination r_j
- During cycles (4), (5) and (6), the next instruction I_{n+1} stalls

Disadvantages during pipelining

- By result forwarding, the next instruction can get the operand result one cycle earlier
- However, there will be still a stall for one clock cycle
- Data dependencies hazard can delay an instruction

Pipeline stall at cycles 5 and 6 for load even with result forwarding at write back stage



Summary

We learnt

- Influence of Simple addressing modes
- Influence of Load and Store Architecture
- Influence of write back in complex addressing Modes

End of Lesson 08 on
Instruction Set Design Influence on Pipelining